A study on high-speed CMOS image sensors and on-sensor image compression circuits

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Application of high-speed videography extends over various fields such as optical scientific measurements and motion analysis. These applications often require image sensors with high sensitivity and high grey-scale resolution. The bottleneck of high-speed image sensors is the data transfer from the sensor chip to an external memory. A solution to this problem is on-sensor image compression. However, because of the very high-image data rate, conventional image compression methods are not suitable for the on-sensor image compression.

This thesis investigates a high-speed CMOS image sensor with a high-sensitivity pixel circuit for global electronic shuttering and a column parallel cyclic 12-bit ADC array, and parallel image compression circuits suitable for integrating on high-speed CMOS image sensors. In order to achieve high-sensitivity, each pixel has a charge amplifier for high-charge-to-voltage conversion, and two sample-and-hold stages for the global shutter. A high-resolution column-parallel cyclic ADC with a built-in noise canceller is proposed. The fabricated chip achieves the full frame rate in excess of 3,500frames/s and 12-bit resolution for the first time as an ADC for high-speed image sensors. The in-pixel charge amplifier achieves the optical sensitivity of 19.9V/lx s. A parallel processing architecture is proposed for on-sensor image compression using a processing element array and a data buffering scheme for parallel data output. The coding efficiency and hardware complexity of several image compression algorithms using 2-D DCT's are compared by means of simulations and logic synthesis and it is revealed that an algorithm with a 4x4-point 2-D DCT, zigzag scanning with 4 blocks, and 1-D Huffman coding is the most suitable for the on-sensor parallel image compression. A possibility of realizing 10,000fps high-speed CMOS image sensor chip with 256 x 256 pixel integrating 16 image compression processing elements is discussed based on logic and layout syntheses, and post-layout simulation. The result shows the effectiveness of the proposed on-sensor image compression circuits for achieving a high-frame-rate image sensor with a reasonable increase in the silicon area.