A Sudy on Dynamic Range Extension Methods and High Resolution Column Parallel Cyclic ADCs for CMOS Image Sensors

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In this thesis, methods to expand a dynamic range of CMOS image sensors and column parallel cyclic ADCs required for high-speed and low noise signal readout have been studied. As a first method to expand the dynamic range of image sensors, a new pixel structure with a pinned photodiode is proposed. In this pixel structure, a pixel response has linear and logarithmic characteristics for the dark and bright regions, respectively. Perfect charge transfer that is required for the linear response in the dark region is verified by using a device simulation. The logarithmic response due to an overflowed charge to expand the dynamic range to the bright region is also confirmed.

Another method to expand the dynamic range of image sensors is based on a high-speed signal readout and multiple exposure technique. Maximally 4 different accumulation time signals are read out at high-speed during one frame period, and are synthesized to reconstruct a wide dynamic image. A prototype image sensor using the high-speed readout of multiple-exposure time signals is developed and evaluated. From the experimental results, the developed image sensor achieves the dynamic range of 153 dB by employing extremely short exposure technique that is shorter than one horizontal readout period. A column-parallel cyclic ADC with high speed and high resolution is an essential building block in order to realize very high-speed signal readout for the multiple-exposure method. A column-parallel cyclic ADC with low-offset and improved-accuracy is proposed, and the measurement result shows that a differential non-linearity (DNL) of 0.3 LSB at 12-bit resolution can be achieved.

For extending the dynamic range of the proposed WDR image sensors into low-illumination region, a low-noise high-resolution cyclic ADC with an improved architecture and digital error calibration method is also proposed. The measured DNL of the prototype ADC is 0.8 LSB at 14-bit resolution, which is the highest resolution as a column-parallel type ADC for CMOS image sensors among column-parallel ADCs ever reported.