A CMOS Image Sensor With In-Pixel Two-Stage Charge Transfer for Fluorescence Lifetime Imaging

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***Abstract*—A CMOS image sensor for time-resolved fluorescence lifetime imaging with subnanosecond time resolution is presented. In order to analyze the fluorescence lifetime, the proposed CMOS image sensor has two charge transfer stages using a pinned photodiode structure in which the first charge transfer stage is for the time-resolved sifting of fluorescence in all the pixels simultaneously and the second charge transfer stage is for reading the signals in each pixel sequentially with correlated double sampling operation. A 0.18-μm CMOS image sensor technology with a pinned photodiode process option is used for the implementation of a 256 $\times$ 256 CMOS image sensor. The decaying images and lifetimes of fura-2 solutions having different concentrations are successfully measured with a 250-ps time step using the CMOS image sensor and ultraviolet laser diode as a light source.**

***Index Terms*—CMOS image sensor, fluorescence lifetime imaging, time-resolved image, two charge transfer stages.**

I. Introduction

FLUORESCENCE techniques have wide applications in medicine and biology for biomolecular detection. However, widely used fluorescence intensity measurements have limitations of the difficulty of quantification and the degradation of the intensity during measurements, so-called photobleaching. To address these limitations and to provide the ability to obtain additional novel information, a fluorescence lifetime imaging microscopy (FLIM) has been intensively studied [1]–[3]. Fluorescence lifetime is defined as an average time prior to returning to the ground state [1]. Different molecules have generally different lifetimes, and even the same molecule in different environments can indicate distinct lifetime [2]. The fluorescence lifetime is one of the most powerful tools to analyze the structures, dynamics, and environments of molecules. For these reasons, the FLIM is studied and applied for many various fields including medical science, biophysics, and biochemistry [3], [4].

A commercial FLIM system uses a time-correlated single-photon counting method using photomultiplier tube detectors and a scanning laser system. The frame rate of this system is limited to 0.001 frames/s for 4096×4096 pixels [5]. A FLIM system with gated image intensifier (GII) and charge-coupled device (CCD) image sensors is also developed. It can be operated at video rate. However, the total system is bulky and expensive. Because of the very small duty ratio in the gating pulse of GII, the availability of light is very small, and the resulting sensitivity is not always high. Recently, time-resolved FLIM systems based on CMOS devices without the need for complex optical systems have been reported [6]–[9]. In [6]–[8], single-photon avalanche diodes in Geiger mode are used for measuring time interval between the light excitation and the arrival of the current pulse due to fluorescent light at the detecting device. In this method, it is difficult to achieve large image array because of complicated circuits for time-to-digital conversions for each pixel. In [9], a differential pixel circuitry with an active reset technique is proposed for time-resolved fluorescence detection. In this approach, the minimum light level is limited by the large circuit noise of 180 electrons.

In this paper, a low-noise video rate CMOS image sensor based on charge modulation technique for the time-resolved FLIM with subnanosecond time resolution is described. The proposed CMOS FLIM sensor has two charge transfer stages using a pinned photodiode structure. The pinned photodiode originally developed for CCD image sensors is now applied for CMOS image sensor to reduce dark current and transfer noise [10], [11], and in this paper, it is applied for resolving fluorescence decaying with high time resolution. For the first stage, a photodiode with shallow potential well is coupled with charge draining and transfer gates. This stage is for sifting fluorescence emission from the excitation light, and time-windowed photodetection and charge transfer. The second stage is for accumulating the sifted charge originated by fluorescence emission and reading the signal. To create the shallow potential well in the first stage using a standard CMOS image sensor technology, the size of photodiode is optimized. The two-stage charge transfer structure cancels the kTC noise, and the resulting noise level is less than 3 electrons. In this device, the duty ratio of the gating pulse width to the cycle time can be arbitrarily chosen and can be optimized for high sensitivity. This is the important difference from the GII of which the minimum cycle time is limited to a few tens of microseconds.

An ultraviolet (UV) periodical pulsed light irradiates fura-2 solution having different concentrations, and the decaying image and lifetime are successfully measured with the CMOS FLIM chip, showing that the time resolution of lifetime measurements is on the order of 100 ps.

The rest of this paper is organized as follows. In Section II, the principle of fluorescence lifetime measurements with the

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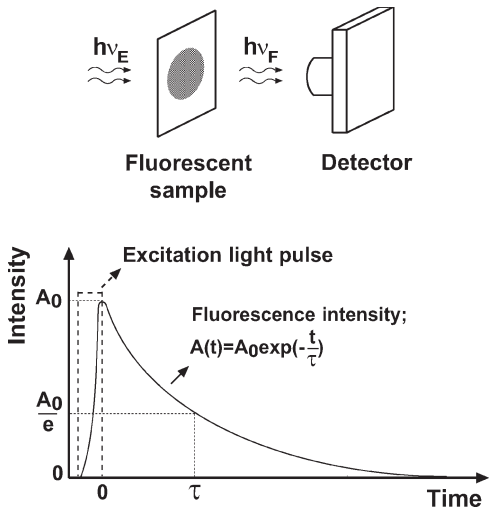

Fig. 1. Typical decay of the fluorescence emission in the time domain. The fluorescence decaying starts with the excitation light "off," and lifetime τ is defined at the time when the fluorescence intensity is A_0/e.

charge modulation technique is described. Section III provides the detailed design and optimization of the pinned photodiodes for FLIM, using device simulations. The measurement results of the implemented CMOS FLIM chip are described in Section IV.

II. Principle of Fluorescence Lifetime Measurement

When a fluorescent sample is illuminated by an excitation light pulse with a very short period of time, fluorescence is emitted with exponential decaying, as shown in Fig. 1. In the case of monoexponential decaying, the fluorescence intensity is given by

$$A(t) = A_0 \exp\left(-\frac{t}{\tau}\right) \tag{1}$$

where A_0 is the initial intensity, and τ is the lifetime of the fluorescence emission.

The fluorescence lifetime is measured with the proposed photodetector using pinned photodiode CMOS image sensor technology, as shown in Fig. 2. A pinned photodiode is connected with a drain and a storage diode, which also has pinned diode structure. The potential well of the photodiode is designed to be shallower than that of the storage diode. Using fringing electric field, electrons are drained or transferred from the photodiode to the drain or storage diode. The draining and transferring speeds of the photodiode are designed to be fast enough for responding to the fluorescence decaying of nanosecond order.

The electron generation in the photodetector, owing to the fluorescence emission, exactly follows the decay of the fluorescence emission. However, detected and stored electrons in the storage diode, as a result of the sifting operation, may have an additional delay and a lifetime deviated from the true fluorescence lifetime, because of the response of the photodetector. Hence, the number of transferred electrons to the storage

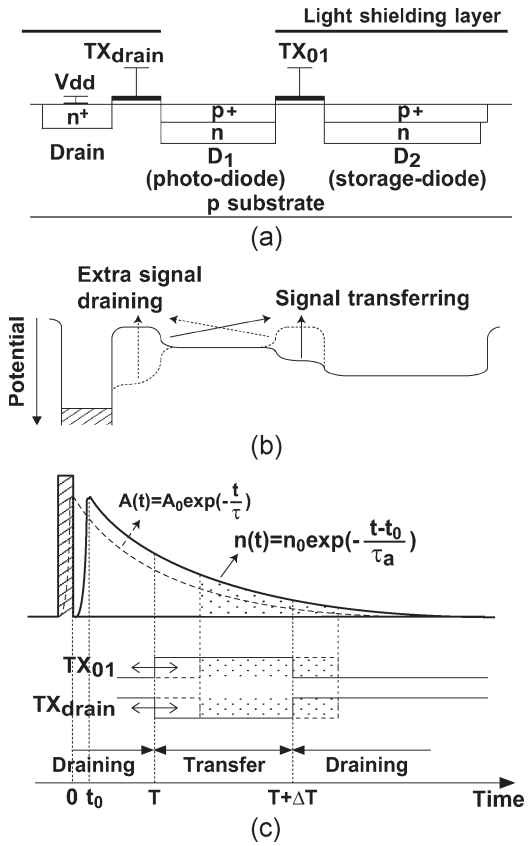

Fig. 2. Structure and principle of the proposed FLIM sensor. (a) Cross-sectional view of the essential part of the proposed pixel structure. (b) Potential profiles of the pixel structure when $TX_{\rm drain}$ and TX_{01} are switched "on." (c) Structure of the time windows and fluorescence decaying. The time windows for draining and transferring have delay time to resolve the fluorescence decaying with high time resolution.

diode per unit time when the transfer gate is opened can be expressed as

$$n(t) = n_0 \exp\left(-\frac{t - t_0}{\tau_a}\right) \tag{2}$$

where n_0 is the initial electron number per unit time, τ_a is the apparent or measured lifetime, and t_0 is the relative delay of the detected electron to the received light. The relationship between the true fluorescence lifetime τ and τ_a is supported to be expressed as

$$\tau_a = \tau + \tau_0 \tag{3}$$

where τ_0 is an offset which is the intrinsic lifetime of the photodetector.

In order to measure the fluorescence lifetime, the transfer gate to storage diode TX_{01} is opened from T to $T + \Delta T$, where T is the delay time of the time window for capturing electrons and ΔT is the width of the time window. The charge draining gate $TX_{\rm drain}$ is opened complementally to the TX_{01} gate. Pulse excitation and fluorescence detection are repeated many times during each integration cycle of the detector in order to intensify the stored electrons, because the signal generated by the fluorescent light due to one-shot excitation light

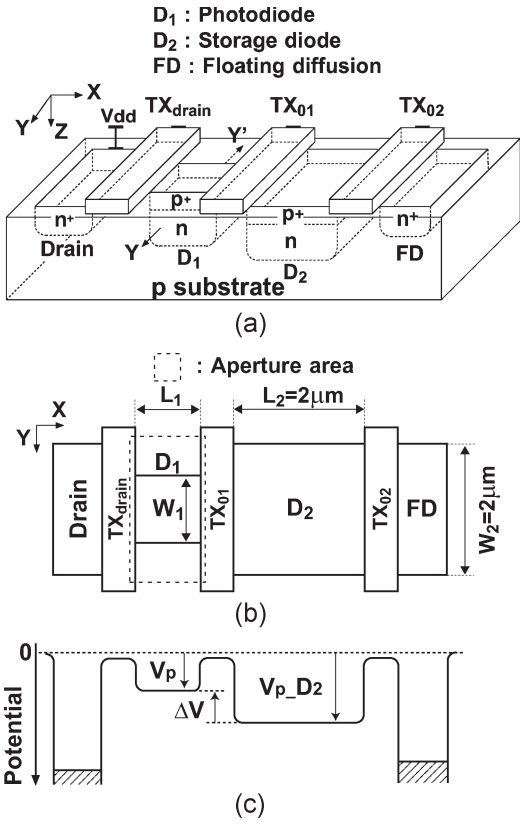

Fig. 3. Schematic overview of the essential part of the pixel structure. (a) Three-dimensional view. (b) X–Y plane layout pattern. (c) Potential profile along X direction.

pulse is very weak. The number of electrons stored in the storage diode is given by

$$N(T) = N_c \int_{T}^{T+\Delta T} n(t)dt$$

$$= \tau_a N_c n_0 \exp\left(-\frac{T-t_0}{\tau_a}\right)\left\{1-\exp\left(\frac{\Delta T}{\tau_a}\right)\right\} \quad (4)$$

where N_c is the number of repeats of irradiations.

Therefore, if $N(T)$ is measured with two different delay times of TX_{01} gate $T = T_1$ and $T = T_2$ $(T_2 > T_1)$, the fluorescence lifetime can be measured by

$$\tau_a = \frac{T_2 - T_1}{\ln\left(\frac{N(T_1)}{N(T_2)}\right)}. \quad (5)$$

III. CMOS FLIM Sensor Design

A. Photodiode Optimization

The device size is optimized by using device simulations. The simulator used is SPECTRA by Link Research Corporation. A typical impurity profile, which is close to that we used in the simulations, is given in [12].

The 3-D view of the essential part of the pixel together with the X–Y plane layout pattern and the potential profile along X direction are shown in Fig. 3. To sift the electrons generated

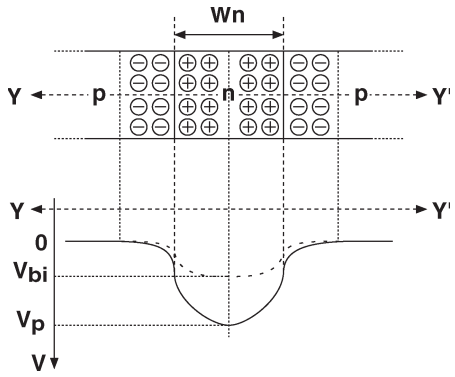

Fig. 4. Electrostatic potential of the fully depleted diode (1-D model).

by only the emitted fluorescence at high speed and without residual electrons, the depth of the potential well V_p of the photodiode D_1 is very important. The potential depth measured from the depth of the potential well $V_p\_D_2$ of the storage diode D_2 is denoted by ΔV. If the impurity concentrations of the n-type region of the photodiode can be controlled independently of that of the storage diode, V_p can be easily controlled. However, in a standard pinned photodiode CMOS image sensor technology, the two different impurity concentrations are not available for the device design. Therefore, the well potential of the photodiode is controlled by the size of the photodiode.

Fig. 4 shows a 1-D model of the fully depleted photodiode. The Y–Y' axis corresponds to that in Fig. 3(a). Using a depletion approximation, the depth of the potential well V_p, which is measured from the p-type substrate when the n-type region is fully depleted, is given by

$$V_p = \frac{1}{8}\frac{q}{\epsilon}N_d\left(1+\frac{N_d}{N_a}\right)W_n^2 \quad (6)$$

where $q = 1.60 \times 10^{-19}$ C is the elementary charge, $\epsilon = 11.8 \times 8.85 \times 10^{-14}$ F/cm is the permittivity of silicon, N_d is the concentration of donors, N_a is the concentration of acceptors, and W_n is the width of the n-type region. The potential well depth can be effectively controlled by the width of the n-type region with a parabolic function. For fully depleting the n-type region, a voltage $V_p - V_{\rm bi}$ is applied at the center of the n-type region, where $V_{\rm bi}$ is the built-in potential. In device simulations, a quasi-Fermi level for electrons in the n-type region is set to larger than $V_p - V_{\rm bi}$ for fully depleting the n-type region. In the following simulation results, a large quasi-Fermi level of 3 V is applied as the initial condition.

Fig. 5 shows the ΔV as a function of the ratio of the photodiode width W_1 to the storage diode width W_2 for four different photodiode lengths normalized by the storage diode lengths L_2 and L_1/L_2 of 0.3, 0.5, 0.75, and 1. The length and width of the storage diode are both 2 μm. As shown in Fig. 5, ΔV can be controlled from 0 to 0.76 V by changing the length and width of D_1.

Fig. 6 shows the charge transfer efficiency as a function of the ratio of W_1 to W_2 for L_1/L_2 of 0.3, 0.5, 0.75, and 1. The transfer efficiency is defined as the ratio of the transferred electrons in D_2 to the electrons in D_1 before transfer. W_1/W_2 and L_1/L_2 are varied from 0.3 to 1 for varying the size.

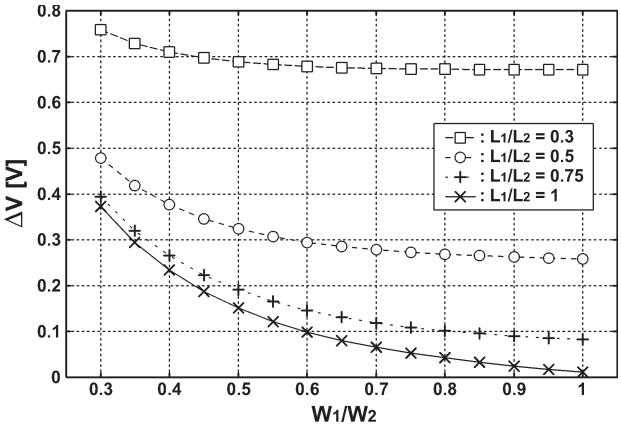

Fig. 5. Simulated potential depth (ΔV) measured from the depth of the potential well of D_2 to that of D_1 as a function of W_1/W_2 for four different sizes of D_1.

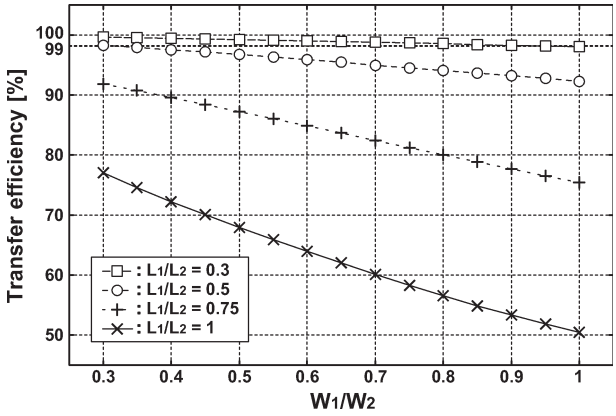

Fig. 6. Simulated transfer efficiency as a function of W_1/W_2 for four different sizes of D_1.

The gate pulse TX_{01} for transferring electrons from D_1 to D_2 is opened for 100 ns. From this simulated result, the transfer efficiency is more sensitive to L_1 than W_1, and if L_1/L_2 is smaller than 0.5, the transfer efficiency of more than 90% can be achieved. The transfer efficiency of more than 99% is obtained for $L_1/L_2 \leq 0.5$ and $W_1/W_2 = 0.3$.

The relationship between τ and τ_a using the two types of D_1 dimensions $L_1/W_1 = 0.6\ \mu$m$/0.6\ \mu$m and $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m is shown in Fig. 7. In this simulation, exponentially decaying light pulses with different time constants are given in the device shown in Fig. 3, and the corresponding apparent lifetimes are calculated by the waveforms of the accumulated electrons in the storage diode. The time step of the simulations is set to 0.25 ns. The intensity of received light is set to 10^{-4} W$/\mu$m^2. The wavelength of the light is 500 nm, which corresponds to that of the peak fluorescence emission of fura-2 solutions used for the experiments described in Section IV. As shown in this simulation results, the apparent lifetime τ_a can be modeled by (3), i.e., the apparent lifetime is bounded by the intrinsic lifetime τ_0 for $\tau \approx 0$ and is expressed as τ for $\tau \gg \tau_0$. Two kinds of dimensions in D_1, which are $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m and $0.6\ \mu$m$/0.6\ \mu$m, do not have large difference in τ_0. From this result, $\tau_0 = 0.62$ ns for D_1 with $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m. Therefore, the lifetime to be

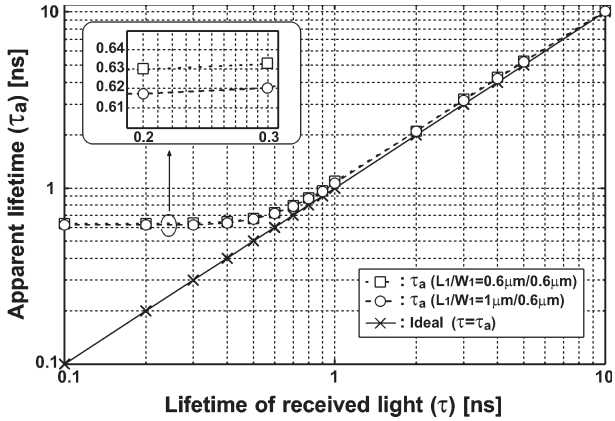

Fig. 7. Relationship between the apparent lifetime (τ_a) calculated with simulation data and the lifetime of the received light (τ) with exponential decaying implemented on a simulator.

measured in the proposed device apparently follows the true fluorescence lifetime in nanosecond order.

Fig. 8(a) shows the τ_a as a function of the initial electron number in D_1, which is controlled by the maximum intensity of input light. From this simulated result, τ_a becomes less dependent on the initial electron number as the initial electron number of D_1 increases. In D_1 with $L_1/W_1 = 0.6\ \mu$m$/0.6\ \mu$m, τ_a is less dependent on the initial electron number when compared with that of D_1 with $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m. However, since the electron generation rate of D_1 with $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m is 13.8 e^-/μW and that of the D_1 with $L_1/W_1 = 0.6\ \mu$m$/0.6\ \mu$m is 4.2 e^-/μW, both have similar dependence of τ_a on the light intensity, as shown in Fig. 8(b).

From the simulation results, the photodiode dimension with $L_1/W_1 = 1\ \mu$m$/0.6\ \mu$m is chosen for the CMOS FLIM sensor, for achieving sufficient measurement accuracy of the lifetime of nanosecond order, and higher sensitivity.

B. Pixel Structure and Operation

Fig. 9 shows the actual pixel structure with potential profiles according to processing steps. The actual photodiode has two fingers for increasing the sensitivity. The two-finger photodiode has almost the same potential distribution along the direction of charge transfer to the storage diode as that of the one-finger type in Fig. 3, since the spacing of the two fingers is chosen such that the V_p of the two-finger photodiode is unchanged from that of the one-finger type. During light illumination for exciting a fluorophore, $TX_{\rm drain}$ is opened for draining the electrons generated by the illuminated light and unwanted fluorescent light, as shown in Fig. 9(a). After draining, TX_{01} is opened for transferring the windowed target electrons, which are generated by only the emitted fluorescence, from D_1 to D_2 as shown in Fig. 9(b). Right after finishing the charge transfer to D_2, $TX_{\rm drain}$ is opened again to remove the residual electrons in D_1 perfectly. These two steps are processed simultaneously at all the pixels for a snapshot real-time imaging. Pulse excitation and fluorescence detection are repeated many times during each integration cycle of the detector, as mentioned before. Finally, as shown in Fig. 9(c), a transfer gate TX_{02} is opened to read out the accumulated fluorescence signals sequentially to the output.

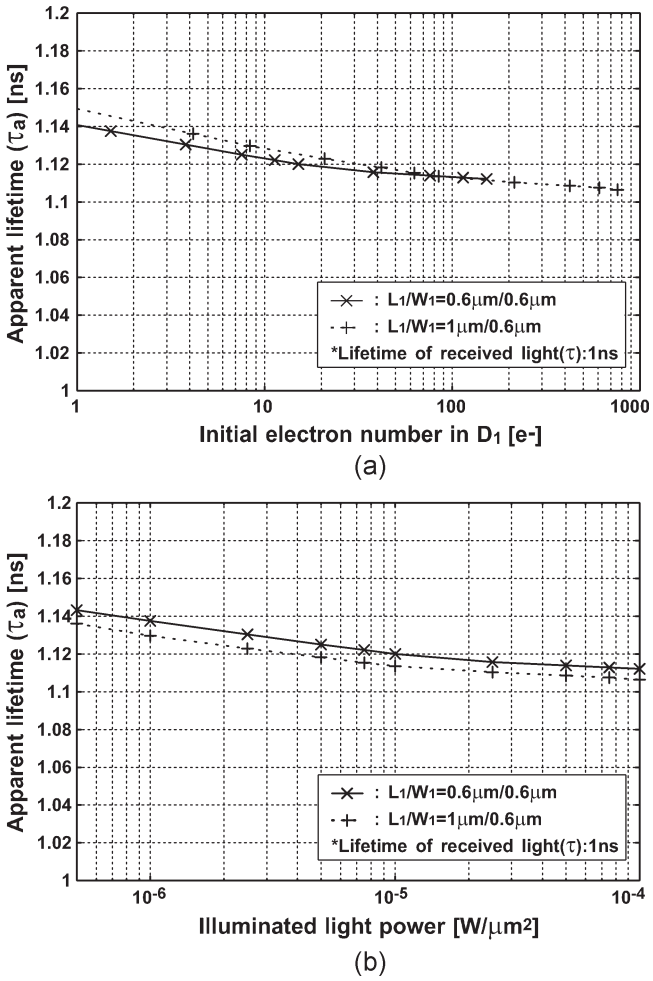

Fig. 8. τ_a calculated with the simulation data (a) as a function of the initial electron number in D_1 and (b) as a function of light power.

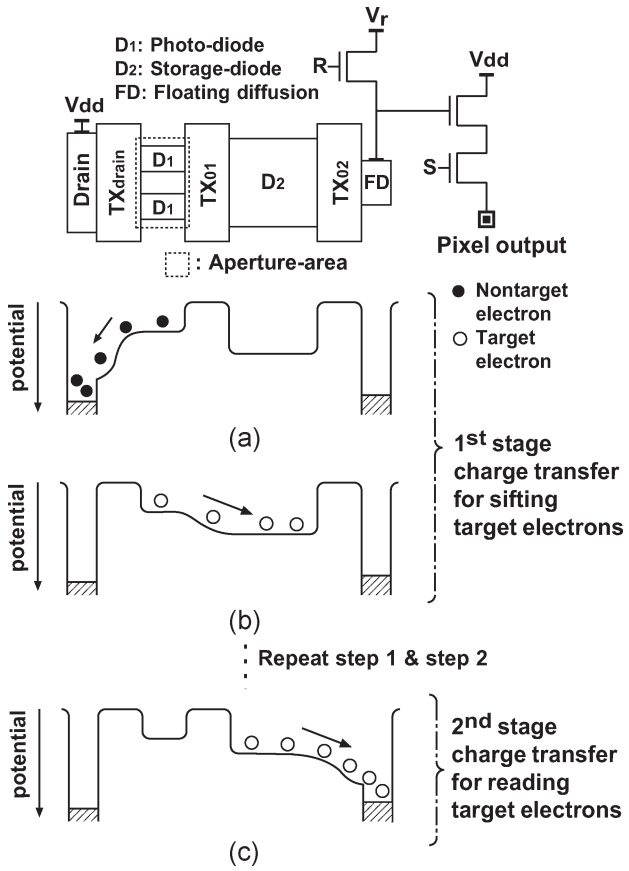

Fig. 9. Implemented pixel structure and potential diagrams for reading fluorescence signal. (a) For draining when $TX_{\rm drain}$ is opened. (b) First stage charge transfer from D_1 to D_2. (c) Second stage charge transfer from D_2 to floating diffusion for reading target electrons. Steps 1 and 2 are repeated many times to intensify the signal electrons.

C. Imager Architecture

Fig. 10 shows the block diagram of the CMOS FLIM chip and timing diagram for the operation. TX_{01} and $TX_{\rm drain}$ gating pulses, of which the starting time is set by the delay time controller, are applied to all pixels simultaneously through gate drivers. The pixel outputs of each row are sequentially fed to a column noise canceling programmable gain amplifier (PGA) with correlated double sampling operation, and the noise canceled signal is read out through horizontal scanning. The gain of PGA, given by the capacitance ratio C_1/C_2, can be set to 1, 2, 4, 8 and 16.

IV. Results and Discussion

A. Implemented Chip

Fig. 11 shows a microphotograph of the CMOS FLIM chip. A four-metal and one-poly 0.18-μm CMOS image sensor technology with a pinned photodiode process option is used. The number of pixels is 256 $\times$ 256, and the pixel size is 7.5 $\times$ 7.5 μm^2. A microlens array is formed on top of the structure.

In order to confirm the linearity and sensitivity of the CMOS FLIM sensor, a photoconversion characteristic with different gains of the PGA is measured using a white light source (66881, Newport) with a color temperature of 3390 K. The transfer gate TX_{01} is always opened, and the transfer gate $TX_{\rm drain}$ is always closed in this measurement. The accumulation time of the photodiode is 32 ms. Fig. 12 shows the measured photoconversion characteristics with gain settings $C_1/C_2 = 1$, 2, 4, 8, and 16. Linear responses are confirmed for all the gain settings. The sensitivity with a gain setting of 16 is 17.5 V/(lx $\cdot$ s).

Because of the parasitic capacitance and the finite open-loop gain of the internal amplifier, the actual gain of the column noise canceling amplifier differs from the capacitance ratio (C_1/C_2) particularly at large gain, as shown in Table I. Using the measured gain, the equivalent number of measured noise electrons is calculated as a function of C_1/C_2, and it is also shown in Table. I. A small noise level of 2.6 e^- is obtained at $C_1/C_2 = 16$.

B. Fluorescence Decaying Image and Lifetime

A measurement system for fluorescence decaying image and lifetime is shown in Fig. 13. For fluorescence materials, fura-2 solutions [13] of different concentrations are used. A UV laser diode (PLP10-038, Hamamatsu Photonics; emission wavelength: 375 nm) is used for exciting fura-2 solutions (peak absorption wavelength: 362 nm; peak emission wavelength: 500 nm). All control pulses are generated by a

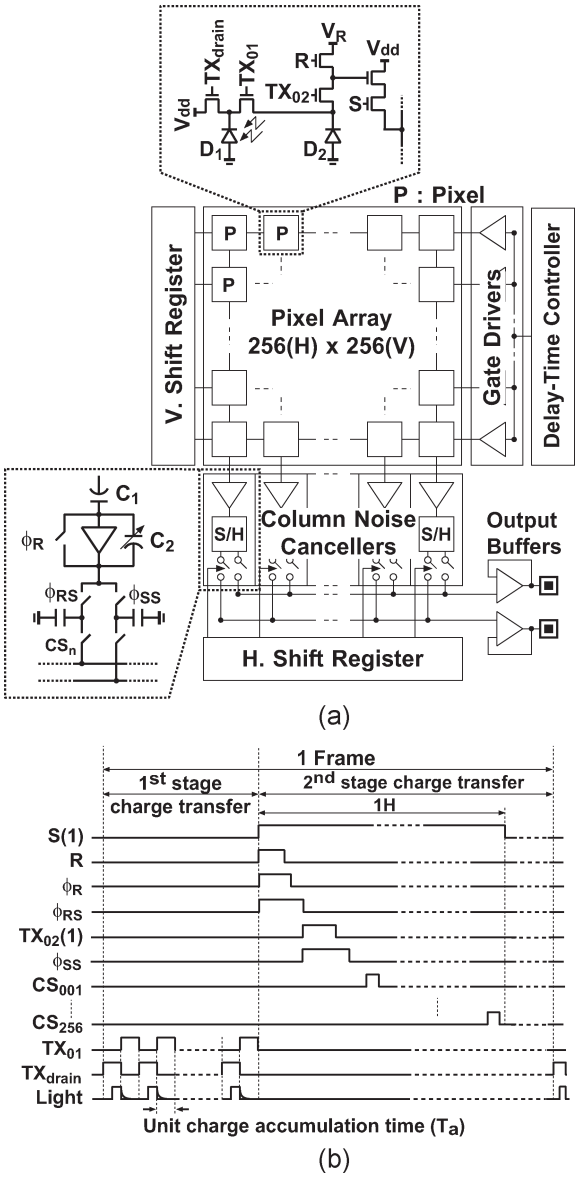

Fig. 10. Block diagram of the CMOS FLIM sensor chip and timing diagram.

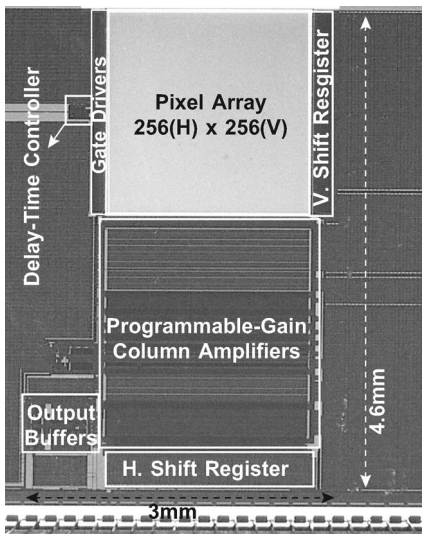

Fig. 11. Chip microphotograph.

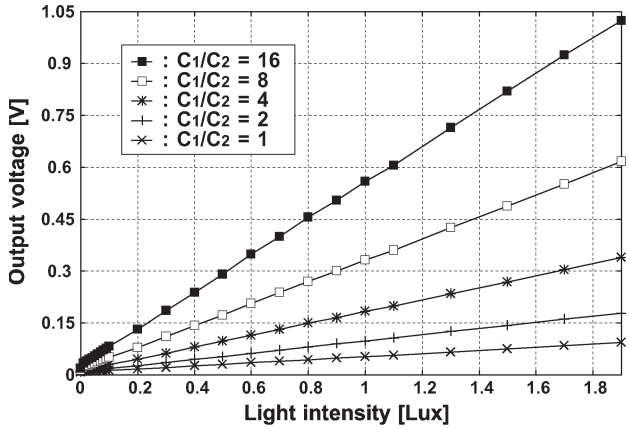

Fig. 12. Linearity and sensitivity of the CMOS FLIM sensor for different column amplifier gain settings.

TABLE I
MEASURED PGA GAIN AND # OF NOISE ELECTRONS

C_1/C_2	Measured gain	# of noise electrons [e^-]
1	1.0	11.4
2	2.0	7.0
4	3.8	4.3
8	7.0	3.1
16	11.8	2.6

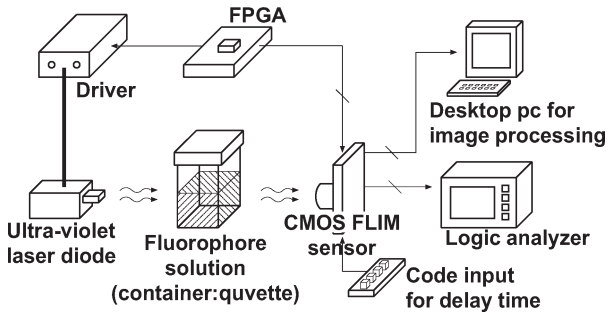

Fig. 13. Measurement system.

field-programmable gate array chip. The signal output is digitized with 14-b analog-to-digital converter, and the output data are stored in a logic analyzer with a large size memory. The digitized output is also fed to a desktop personal computer for image processing. The decay time of the time window for fluorescence detection can be set by internal and external delay controllers with a 250-ps resolution. The time window is set to 500 ns. The gain of PGA, C_1/C_2, is set to 16. The pixel readout rate is 2 MHz for the video imaging at 30 frames/s.

The measurement results of fluorescence decaying of the fura-2 solutions and the decay of the UV laser diode are shown in Fig. 14. The concentration of the fura-2 solutions is varied from 10 to 50 nmol. The decaying of UV laser diode is smaller than 50 ps. The measured decaying for UV laser diode shows a lifetime of 0.7 ns, which corresponds to the intrinsic lifetime τ_0 of the CMOS FLIM sensor. The measured τ_0 is relatively close to the simulation results in Fig. 7. The intensity of the fluorescence emission finally approaches to zero. However, the signal electrons do not approach to zero. This is due to signal components with slow response, mainly caused by

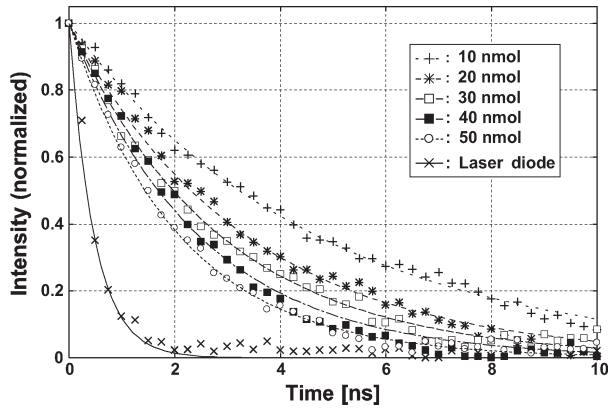

Fig. 14. Measured fluorescence signal intensity (after offset canceling) of fura-2 solutions as a function of the delay time of capture window (linear scale).

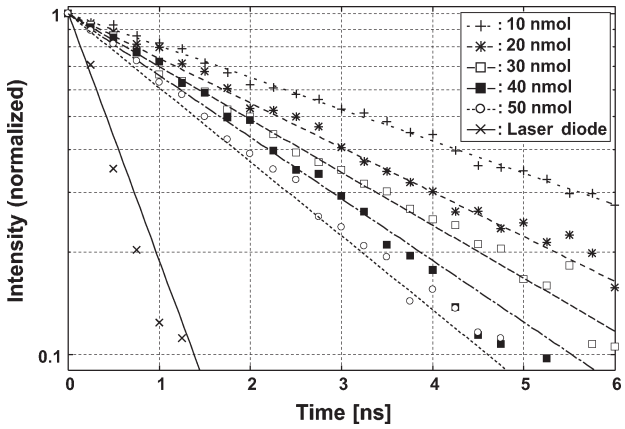

Fig. 15. Measured fluorescence signal intensity (after offset canceling) of fura-2 solutions as a function of the delay time of capture window (log scale).

electron traps at Si–SiO_2 interface under the transfer gate. The trapping and detrapping at Si–SiO_2 interface states may cause an image lag in conventional image sensors. However, in the CMOS FLIM sensor, the trapping and detrapping cause an offset, because the average time of detrapping from the Si–SiO_2 interface state is much larger than the lifetime of fluorescence decaying of nanosecond order. Hence, for more accurate lifetime calculation, the number of electrons per unit time generated by fluorescence emission, denoted by $n(t)$ in (2), is redefined as

$$n(t) = n_0 \exp\left(-\frac{t - t_0}{\tau_a}\right) + n_B \tag{7}$$

where n_B is the number of offset electrons per unit time. Therefore, the apparent or measured lifetime is also modified to

$$\tau_a = \frac{T_2 - T_1}{\ln\left(\frac{N(T_1) - N(T_3)}{N(T_2) - N(T_3)}\right)} \tag{8}$$

where T_3 is the delay time when the fluorescence decaying signal becomes much smaller than the offset. Fig. 15 shows a plot for log intensity versus time after offset canceling. This shows that the measured response agrees well with the monoexponential decaying of fluorescence emission.

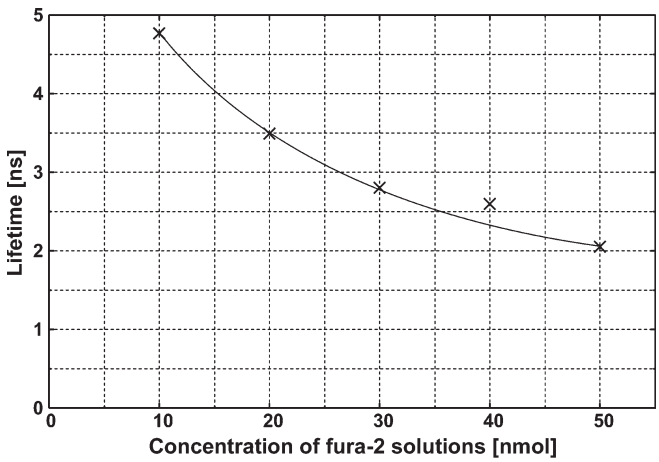

Fig. 16. Measured lifetimes of fura-2 solutions using the CMOS FLIM sensor.

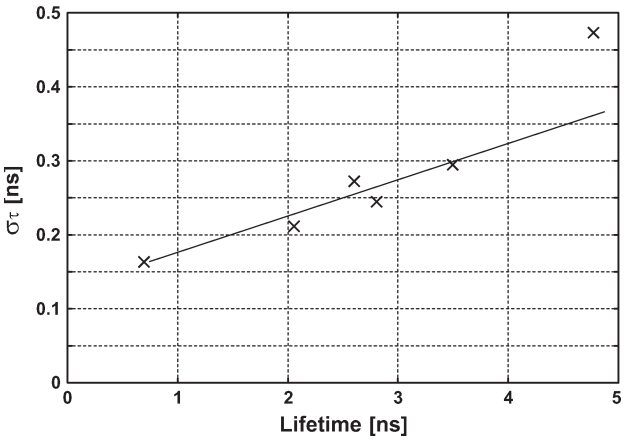

Fig. 17. Standard deviation (σ_τ) of the measured lifetimes.

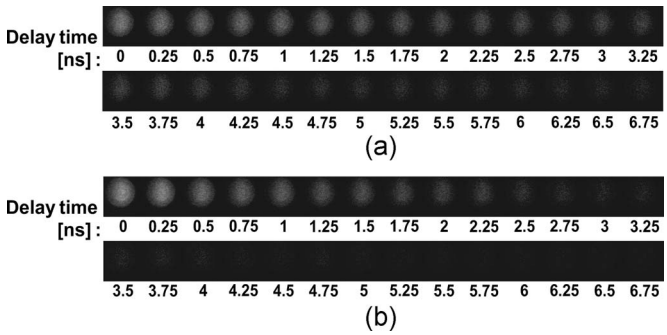

Fig. 18. Snapshot images of fluorescence decaying for (a) 10 and (b) 40 nmol of the fura-2 solutions.

The lifetimes of different fura-2 concentrations calculated using (8) are shown in Fig. 16. The standard deviation σ_τ of the measured lifetimes is shown in Fig. 17. σ_τ depends on the lifetime, and it is 160 ps for a measured lifetime of 0.7 ns.

Fig. 18 shows the decaying images with a 250-ps time step for two concentrations of fura-2 solutions: 10 and 40 nmol. It is observed that the decaying of the lower concentration of fluorescence solution is obviously slower than that of the higher concentration one. This is the first result to show that the CMOS-based FLIM system can observe the imaging of the decaying process of the fluorescence emission.

V. Conclusion

A CMOS image sensor with in-pixel two-stage charge transfer for a time-resolved FLIM is presented in this paper. The sensor chip with 256 $\times$ 256 pixels has been implemented in a 0.18-μm CMOS image sensor technology with a pinned photodiode process option. The two-stage charge transfer structure allows one to realize time-resolved fluorescence detection of subnanosecond time resolution, sifting the fluorescence signal from the excitation signal, and low-noise signal readout with kTC noise canceling. The fluorescence lifetime of nanosecond order and the decaying image with a 250-ps time step have been successfully measured. The application of the developed FLIM sensor to biological samples is left as a near future subject.

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References

[1] J. R. Lakowic, *Principles of Fluorescence Spectroscopy*, 3rd ed. New York: Springer-Verlag, 2006.

[2] X. F. Wang and B. Herman, *Fluorescence Imaging Spectroscopy and Microscopy*. Hoboken, NJ: Wiley, 1996.

[3] D. Elson, S. Webb, J. Siegel, K. Suhling, D. Davis, J. Lever, D. Phillips, A. Wallace, and P. French, "Biomedical applications of fluorescence lifetime imaging," *Optics Photonics News*, vol. 13, no. 11, pp. 26–57, Nov. 2002.

[4] T. Oida, Y. Sako, and A. Kusumi, "Fluorescence lifetime imaging microscopy (flimscopy)," *Biophys. J.*, vol. 64, pp. 676–685, Mar. 1993.

[5] *Time Correlated Single Photon Counting Systems*. [Online]. Available: http://www.boselec.com/TCSPCSystems12-29-04.pdf.pdf

[6] D. E. Schwartz, E. Charbon, and K. L. Shepard, "A single-photon avalanche diode imager for fluorescence lifetime applications," in *Proc. Dig. Tech. Papers, Symp. VLSI Circuits*, 2007, pp. 144–145.

[7] F. Borghetti, D. Mosconi, L. Pancheri, and D. Stoppa, "A CMOS single-photon avalanche diode sensor for fluorescence lifetime imaging," in *Proc. Int. Image Sensor Workshop*, Jun. 2007, pp. 250–253.

[8] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 $\times$ 128 single-photon imager with on-chip column-level 10 b time-to-digital converter array capable of 97 ps resolution," in *Proc. Dig. Tech. Papers, Int. Solid State Circuits Conf.*, Feb. 2008, pp. 44–45.

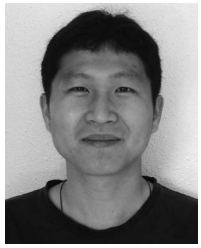
[9] T. Huang, S. Sorgenfrei, K. L. Shepard, P. Gong, and R. Levicky, "A CMOS array sensor for sub-800-ps time-resolved fluorescence detection," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 829–832.

[10] N. Teranishi, A. Kohno, Y. Ishihara, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor," in *IEDM Tech. Dig.*, Dec. 1982, pp. 324–327.

[11] P. P. K. Lee, R. C. Gee, R. M. Guidash, T.-H. Lee, and E. R. Fossum, "An active pixel sensor fabricated using CMOS/CCD process technology," presented at the IEEE Workshop Charge Couple Device Advanced Image Sensors, Dana Point, CA, Apr. 1995.

[12] A. Krymski and K. Feklistov, "Estimates for scaling of pinned photodiodes," in *Proc. IEEE Workshop CCD AIS*, 2005, pp. 60–63.

[13] S. M. Keating and T. G. Wensel, "Nanosecond fluorescence microscopy. Emission kinetics of fura-2 in single cells," *Biophys. J.*, vol. 59, no. 1, pp. 186–202, Jan. 1991.



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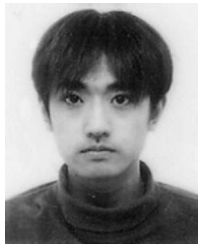

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