Single-Electron Transfer by Inter-Dopant Coupling Tuning in Doped Nanowire Silicon-On-Insulator Field-Effect Transistors

Daniel Moraru, Maciej Ligowski, Kiyohito Yokoi, Takeshi Mizuno, and Michiharu Tabe[a)]

Research Institute of Electronics, Shizuoka University,

3-5-1 Johoku, Nakaku, Hamamatsu 432-8011, Japan

Abstract

We demonstrate tunable single-electron turnstile operation in doped-nanowire silicon-on-insulator field-effect transistors. In these structures, electron transport occurs through dopant-induced quantum dots. We show that the substrate silicon can be used as a back gate to modulate the inter-dot coupling, which dictates the overlap between Coulomb domains in the charge stability diagrams of these devices. Since this overlap is a necessary requirement for single-electron turnstile, this procedure allows the optimization of the conditions for single-electron turnstile in doped-nanowire field-effect transistors.

[a)]Email address: romtabe@rie.shizuoka.ac.jp

Single-electron transfer operation is attractive for future electronics since it would allow a significant power consumption reduction for logic and memory devices. Single-electron turnstile, consisting of a chain of three metallic quantum dots (QDs) with a single ac gate coupled to the central one, is the simplest device design that can be used for this operation.[1] In these devices, individual electrons are transferred from source to drain during every cycle of the ac gate voltage under a finite source-drain bias.

From a practical viewpoint, silicon devices are preferable for single-electron transfer. It has been demonstrated that single-dot single-electron transistors (SETs) can operate as multi-gate single-electron transfer devices.[2] However, for that purpose, two phase-correlated ac gates were used to control the conductance of the two tunnel barriers connecting the dot to the leads. More recently, we have demonstrated that single-electron turnstile can be achieved in doped silicon nanowire SETs made in silicon-on-insulator (SOI) substrates using only one ac gate.[3,4] Under ac operation, in some devices individual electrons were transferred one at a time between leads through the irregular potential landscape created by discrete dopants. In these devices, QDs are formed by individual dopants or clusters of dopants and not by lithographic techniques. Unfortunately, the uncontrolled doping leads to variations from device to device of dopants positions, which may affect the ability of some devices to be used for single-electron turnstile operation. Recently, techniques have been developed for achieving more control over dopant distribution[5] and for monitoring the dopant-induced potential profile in silicon nanodevices.[6]

Different from the above mentioned approaches, in this work we propose a technique for electrically adjusting the conditions necessary for single-electron turnstile in conventionally doped nanowire SETs. One of the conditions is an appropriate overlap of stable charge domains (Coulomb diamonds) in the stability diagram.[7] This overlap depends on the inter-dot coupling

strength, becoming smaller as coupling increases. Therefore, it is important to control the inter-dot coupling in order to achieve single-electron turnstile conditions. For that purpose we propose a method based on particular characteristics of doped-nanowire SOI-SETs: natural misalignment of dopants incorporated in the conduction path and availability of a back gate (substrate Si layer) for applying strong electric fields across the channel. Recently, the possibility of controlling inter-dot coupling using back gate has been demonstrated in few-electron double quantum dots in carbon nanotubes.[8]

The devices investigated in this work are nanowire SOI-FETs, with a structure schematically shown in Fig. 1(a). The top silicon layer was first uniformly n-type doped with phosphorus diffused from a spin-coated silica film containing phosphorus oxide (P_2O_3). Dopant activation was done by thermal annealing at 1000°C for 20 minutes. The concentration estimated from room temperature four-point probe measurements and from SIMS measurements on thick-Si reference samples doped with the same process was found to be $N_d \approx 1\times10^{18}$ cm^{-3}. It is expected that the average inter-dopant spacing of $N_d^{-1/3} \approx 10$ nm. This is larger than the Bohr radius for phosphorus in silicon (≈3 nm),[9] suggesting that single dopants may be the origin of QDs in this system. The nanowire constriction channel was then defined by an electron beam lithography technique to have a length of 100 nm and an effective width of about 50 nm. The final thickness of the top Si layer, after gate oxide growth (t_{ox}=10 nm), was estimated to be t_{Si}=7 nm. An aluminum front gate was deposited covering the channel as well as the wider pads towards source and drain. The advantage of the SOI structures is that the channel is also coupled to the substrate Si through a 400 nm-thick buried oxide layer. In this work, we will use this additional back gate voltage (V_{bg}) as a parameter to modulate the inter-dot coupling. Although it is estimated that there should be about 50 dopants in the constriction channel, it is expected that a

lowest-potential path will be formed along the central axis of the channel due to the long-range action of ionized dopant potentials. Therefore, a one-dimensional array of dopant-induced QDs will control the transport through these devices.[10]

The I_{sd}-V_{fg} characteristics measured for one doped-nanowire SET at a source-drain bias V_{sd}=10 mV and back gate voltage V_{bg}=0 V are shown in Fig. 1(b). Current oscillations can be observed indicating the fact that transport is governed by the Coulomb blockade effect. The split-peak features suggest that a multiple-dot array is formed within the channel.[11] This is expected due to the axial symmetry of the potential inside the constriction channel. More importantly, the fact that the first peak is split into three sub-peaks is an indication that transport may occur through a 3-QD array at the initial stages of the conduction for this particular device. This is in good agreement with our simulations of surface potential profile for 100×50×10 nm^3 channels, as shown in Fig. 1(c). In these simplified simulations, we consider that individual dopants introduce each a Coulombic potential well.[10] Dopants are placed randomly in the volume of the channel and the potential is obtained as the result of the superposition of Coulombic potential wells due to all the dopants. The effects of free electrons screening the dopant-induced potential profile have not been considered. We suggest that this provides a reasonable picture of the channel potential for the V_{fg} region of interest in our study, i.e., close to threshold. For these conditions, negative V_{fg} is expected to deplete free carriers from the channel. It can be observed from the simulated potential profile that there are several global potential minima (indicated by circles) along the channel. These minima will act as initial QDs at the early stages of the conduction (close to the threshold), most probably giving rise to the first peaks in the I_{sd}-V_{fg} characteristics.

Finding a procedure to tune the coupling between these initial dopant-induced QDs would allow an optimization of the transport characteristics for single-electron transfer operation. We suggest that back gate can be used in our SOI-SET structures as a tuning gate. For illustrating the tuning principle, we take the simple case of a 3QD array in which the dots contain single dopants vertically misaligned (marked as A, B, and C). Such conditions may occur due to the uncontrolled doping technique and irregular potential landscape inside the channel. This case is shown in Fig. 1(d). The tuning principle described next can be easily generalized for other dopant arrangements as well. When no back gate voltage is applied [Fig. 1(d1)], we can assume that the bottoms of the three dopant-induced potential wells are energetically aligned so that electrons injected in the channel from source see a specific configuration of QDs and tunnel barriers (marked by blue dashed lines). By applying a finite back gate voltage two effects are expected to take place. First, the whole potential in the channel will be raised or lowered, depending on the polarity of V_{bg}. This shift of the channel potential relative to the source Fermi level can be compensated by applying an additional front gate voltage (V_{fg}) of opposite polarity to V_{bg}. Second and more important, V_{bg} application will introduce an additional electric field vertically across the channel, which cannot be compensated by V_{fg} application. As a consequence, the dopants in the conduction path, located at different positions across the channel thickness, will be affected differently by the additional electric field introduced by V_{bg}. The potential profile will be modified as illustrated in Fig. 1(d2). This means that the effective barrier thickness between the dopant-dots (which is a measure of inter-dot coupling) will be modulated by the back gate voltage V_{bg}, as indicated by the red dashed lines.

Figures 2(a), (b), and (c) show the stability diagrams measured at 17 K for three different values of V_{bg}: 0, -5, and -10 V, respectively. These diagrams contain series of diamond-shaped

zero-current regions (Coulomb diamonds). For the ranges of V_{fg} and V_{sd} delimiting these diamonds electron transport is blockaded with a specific number of electrons trapped inside the QD array. The number of charges expected to be found in the system is indicated inside each Coulomb diamond. It can be observed that by increasing V_{bg} the structure of the stability diagrams is significantly changed. For V_{bg}=0 V, the individual diamonds can be hardly distinguished from each other due to the strong overlap (for instance, diamonds labeled 2, 3, 4 in Fig. 2(a)). For V_{bg}=-5 V, the diamonds start to separate from each other, which is already an indication of the change in inter-dot coupling (Fig. 2(b)). This effect is even more pronounced for V_{bg}=-10 V for which case most diamonds in the stability diagram can be distinctly observed, without significant overlaps, as can be seen in Fig. 2(c). This is a signature that the system starts to behave as a single-dot device. This can be ascribed to a strong enhancement of inter-dot coupling which makes the dopant-induced QDs eventually merge into a larger dot. Another possible reason would be conduction path change by changing V_{bg}. Such changes are expected to occur as V_{fg} increases due to the limited occupancy of each dopant-induced QD. However, the systematic changes of the structure of the stability diagrams shown in Figs. 2(a)-(c) suggest that conduction path is not changed as a function of V_{bg} for Coulomb diamonds corresponding to a certain number of charges trapped in the system. Therefore, changes in the QD array parameters such as inter-dot coupling should be responsible for the modifications in the stability diagrams.

For analyzing single-electron transfer, we focus on the left-most Coulomb domains shown in Figs. 3(a)-(c). Guides for the eyes are drawn to roughly delineate the expected boundaries between the consecutive domains. These domains are most important for single-electron turnstile operation because of their large extension in V_{sd}. For these two regions it can be also noticed that the overlap is modified by V_{bg}, from a strong overlap for V_{bg}=0 V to a very

weak one for V_{bg}=-10 V. Optimal conditions correspond to the case of V_{bg}=-5 V for which an overlap centered at V_{fg}=-0.4 V is extending up to higher V_{sd}. At the same time, wide ranges of V_{fg} are available inside the stable domains on the left and right sides of the overlap, which allows us to set the low and high levels of the ac V_{fg} pulse with sufficient certainty. For the other V_{bg} cases, identification of suitable conditions for single-electron transfer is practically impossible.

Figure 3(d) shows ac I_{sd}-V_{sd} characteristics (f=1 MHz) for each V_{bg} case obtained by setting a V_{fg} pulse with 50 mV peak-to-peak amplitude. The offset value was fixed inside the overlap between adjacent Coulomb diamonds, as indicated by the vertical dashed lines. As a criterion for single-electron turnstile operation, plateaus at $I_{sd}=e\times f$ should be observed in the ac I_{sd}-V_{sd} characteristics.[1] The curves for V_{bg}=0 V and -10 V do not exhibit any such features and therefore, under these conditions, the device does not work as a single-electron transfer device. By optimizing the inter-dopant coupling, as done by setting V_{bg} at -5 V, the obtained curve shows the expected plateau extending for about 40 mV in V_{sd}. For this condition, during every cycle of the ac V_{fg} one electron is transferred from source to drain and thus single-electron turnstile is realized. It should be noted that the current level in the plateau region is slightly larger than $e\times f$ due to small leakage current or thermally-activated tunneling events (T=17 K). Figure 3(e) shows the frequency dependence of I_{sd} (averaged for a range of 20 mV inside the observed plateaus) under ac V_{fg} application. Current in the plateau region is proportional to operation frequency ($I_{sd}\approx e\times f$) confirming that the plateau is due to single-electron turnstile operation. A slight dependence on duty time has been also observed.

In summary, tuning of inter-dot (inter-dopant) coupling in doped-nanowire SOI-FET was demonstrated using the back gate voltage. This allowed the control of the overlap between

Coulomb diamonds in the stability diagrams. Based on this tuning procedure, the overlap was properly adjusted and single-electron transfer (turnstile) operation could be achieved.

The authors thank D. Nagata for support during experiments and H. Ikeda for helpful discussions. This work was partially supported by Grants-in-Aid for Scientific Research (16106006 and 18063010) from the Ministry of Education, Culture, Sports, Science, and Technology.

References

[1]L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64**, 2691 (1990).

[2]Y. Ono, N. M. Zimmerman, K. Yamazaki and Y. Takahashi, Jpn. J. Appl. Phys. **42**, Part 2, L1109 (2003).

[3]D. Moraru, Y. Ono, H. Inokawa, and M. Tabe, Phys. Rev. B **76**, 075332 (2007).

[4]K. Yokoi, D. Moraru, M. Ligowski, and M. Tabe, Jpn. J. Appl. Phys. **48**, 024503 (2009).

[5]T. Shinada, S. Okamoto, T. Kobayashi, and I. Ohdomari, Nature (London) **437**, 1128 (2005).

[6]M. Ligowski, D. Moraru, M. Anwar, T. Mizuno, R. Jablonski, and M. Tabe, Appl. Phys. Lett. **93**, 142101 (2008).

[7]H. Ikeda and M. Tabe, J. Appl. Phys. **99**, 073705 (2006).

[8]G. A. Steele, G. Gotz, and L. P. Kouwenhoven, Nature Nanotechnol. (in print).

[9]S. R. Schofield, N. J. Curson, M. Y. Simmons, F. J. Rueß, T. Hallam, L. Oberbeck, and R. G. Clark, Phys. Rev. Lett. **91**, 136104 (2003).

[10]G. J. Evans, H. Mizuta, and H. Ahmed, Jpn. J. Appl. Phys., Part 1 **40**, 5837 (2001).

[11]F. R. Waugh, M. J. Berry, D. J. Mar, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Phys. Rev. Lett. **75**, 705 (1995).

Figure captions

FIG. 1. (a) Device structure of doped-nanowire SOI-FETs. Al front gate and silicon substrate (back gate) can control the potential inside the doped constriction channel. (b) Dc I_{sd}-V_{fg} characteristics measured for one doped-nanowire SET. The first observable group of peaks is marked and the sub-peaks are indicated by red circles. (c) Potential profile simulated for a $100\times50\times10$ nm^3 channel for a doping concentration $N_d\approx1\times10^{18}$ cm^{-3} (global minima are also marked). (d) Schematic depiction of a nanowire with three dopant-induced QDs and the modulation of inter-dot coupling by applying finite back gate voltage V_{bg}.

FIG. 2. (a)-(c) Measured stability diagrams for V_{bg}=0, -5, and -10 V, respectively, with stable states labeled from 0 to 7 (according to the expected number of electrons in the array).

FIG. 3. (a)-(c) Extracts from the stability diagrams shown in Figs. 2(a)-(c), respectively, for V_{bg}=0, -5, and -10 V. Guides for the eyes are roughly drawn to indicate the overlap between the $n_{\sum}$=0 and $n_{\sum}$=1 stable regions. (d) ac I_{sd}-V_{sd} characteristics for V_{bg}=0, -5, and -10 V. Single-electron transfer features can be observed only for the case of V_{bg}=-5 V as an $e \times f$ plateau extending for a wide range of V_{sd}. (e) Frequency dependence of average I_{sd} estimated inside the plateau (V_{sd}=50~70 mV range) for ac V_{fg}. Standard deviation is also shown as error bars.

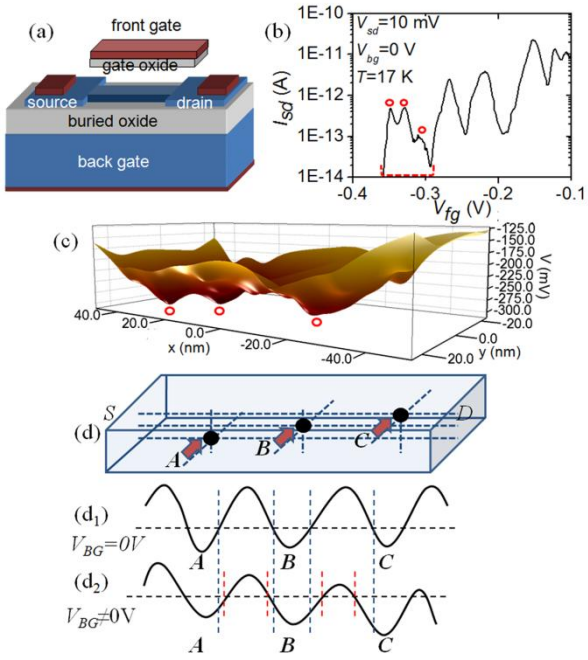

FIG. 1. D. Moraru *et al.*, APEX

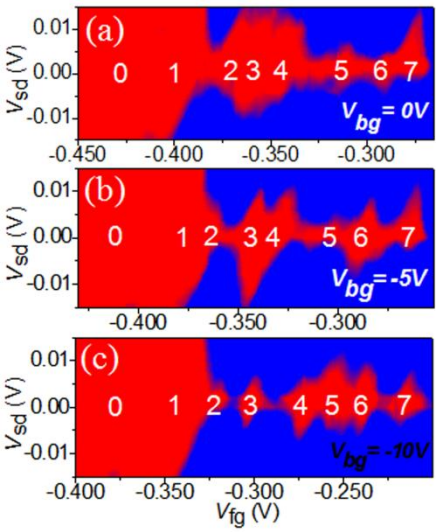

FIG. 2. D. Moraru *et al*., APEX

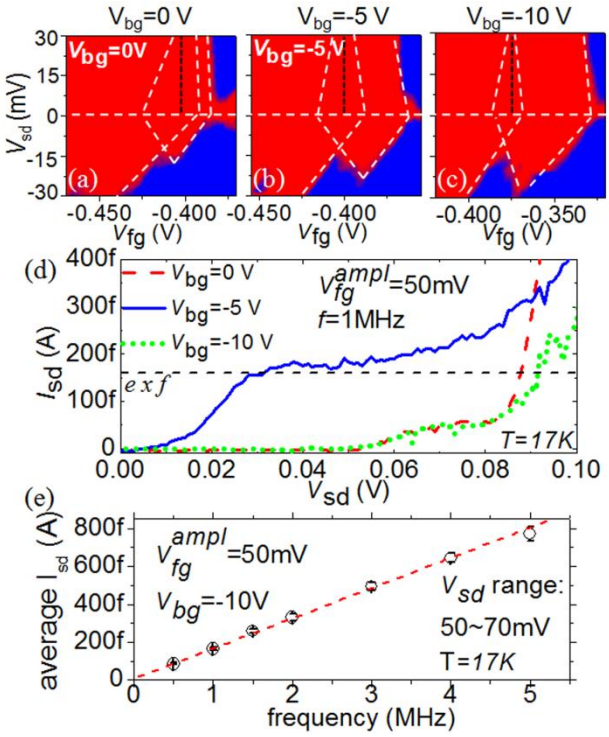

FIG. 3. D. Moraru *et al.*, APEX