Single-Gated Single-Electron Transfer in Non-Uniform Arrays of Quantum Dots

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Single-electron transfer operation in single-gated one-dimensional quantum dot arrays is investigated statistically from the viewpoint of robustness against parameter fluctuations. We have found numerically that inhomogeneous quantum dot arrays as formed in doped nanowires exhibit single-electron transfer in a wide range of parameters. This confirms our frequent experimental observation of single-electron transfer in doped-nanowire field-effect transistors. The most important result in this work is that three-dot arrays with small-large-small dot size distribution always allow single-electron transfer even under dot size fluctuations. This structure is, we believe, most promising for fabricating devices with high immunity against structural fluctuations in nanometer-scale. Finally, based on these findings, we propose methods to fabricate high-yield single-electron transfer devices.

KEYWORDS: Coulomb blockade, single-electron transfer, individual dopants, inhomogeneous quantum dot arrays, Monte Carlo simulation

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1. Introduction

Control of charge at the elementary level has become possible within the last decades due to the emergence of a new class of electronic devices: single-electron transistors (SETs).[1] SETs contain one or more small conductive regions (so-called Coulomb islands or quantum dots) weakly coupled to each other and to the leads through tunnel junctions. These devices operate based on single-electron tunneling and Coulomb blockade effect that occurs when electrons localized on the islands block the current flow for a significant range of applied voltages. A variety of applications can be envisaged for SETs, including but not limited to low-power-consumption very-large-scale-integration (VLSI) circuits,[2] sensitive electrometers,[3] or metrological standards.[4] One of the building blocks for these applications is a single-electron transfer device, i.e., an SET able to transfer sequentially in time individual electrons synchronized with external gate pulses.

Several designs for single-electron transfer devices have been proposed in the early 1990's, such as single-electron turnstiles[5] and single-electron pumps[6] using one-dimensional (1D) arrays of metallic quantum dots (QDs). There are several limitations of these metallic single-electron transfer devices: high sensitivity to background charge fluctuations, limited operation temperature (~100 mK) and incompatibility with present complementary metal-oxide semiconductor (CMOS) technology. For practical applications, it is useful to realize single-electron transfer in semiconductor devices. In this direction, single-electron turnstile operation has been already demonstrated using single-island SETs made in GaAs/AlGaAs heterostructures[7] and, more recently, in silicon single-dot SETs.[8] The operation principle of these semiconductor-based devices is different from that of the original turnstile device.

Single-electron transfer is achieved by modulating the conductance of the two tunnel junctions that couple the dot to the leads using two phase-correlated ac-gates.

Replacing the single island with multiple-QD arrays is promising for achieving higher operation temperatures[9)] and better stability against cotunneling effects.[10)] Furthermore, controlling single-electron transfer with only one ac-gate is desirable from the viewpoint of simplicity of the biasing circuit. Fabrication of multi-dot arrays in silicon at nanometer scale is, however, not a trivial task. Several methods have been demonstrated so far for fabricating silicon multiple-QD arrays and devices comprising such multi-dot structures exhibited Coulomb blockade features at fairly high temperatures (~100 K).[11-13)] Although experimental evidence of controlled single-electron transfer in such devices is still lacking, it has been numerically proved that two-dimensional (2D) multiple-QD arrays in a single-gated field-effect transistor (FET) structure can work as single-electron turnstile devices under specific conditions.[14)] Systems with smaller total capacitance are desirable for improving the device operation but the reduction of tunnel junctions and QD sizes meets a barrier in the present limitations of lithographic techniques. These limits can be overcome by utilizing individual dopants rather than lithographically-defined QDs as elementary charge confinement centers. An ionized donor, for instance, introduces a Coulombic potential well that acts as a QD for electrons with the spatial extension on the order of the Bohr radius for phosphorus in Si (about 3 nm).[15-18)] These dimensions are smaller than the spatial resolution currently achievable by lithography. Impurity doping of Si is a well characterized process for bulk Si, although the control of the dopant location to individual dopant level remains an important challenge. Taking into account the uncontrollability of dopant distribution, it should be thus expected that dopant-induced QD

arrays obtained by conventional doping techniques are essentially inhomogeneous, strongly depending on the number and positions of dopants in the device channel.

We have suggested that inhomogeneity can be useful in promoting one-directional transfer of elementary charges under the action of a single gate. In our previous studies of single-gated doped-nanowire FETs, we have in fact frequently observed single-electron transfer operation features (plateaus in the ac I_{sd}-V_{sd} characteristics aligned at ef current level, where e is the elementary charge and f is the ac operation frequency).[19] Thus, we have already shown that random dopant arrays are generally capable of realizing single-electron transfer with a simple biasing circuit. These findings are still surprising because the QD arrays contained in these devices are not precisely designed, but naturally formed by individual dopants.

In this study, we mainly focus on the feasibility of dopant-induced QD arrays as single-electron transfer devices from the viewpoint of robustness against fluctuations of device parameters (mainly dot size dispersion). For this purpose, we performed extensive Monte Carlo simulations (using a procedure similar to our previous studies[14,19]) of electron transport for 1D inhomogeneous QD arrays for a statistical number of QD configurations and taking into analysis a wide range of parameters. Our final goal was to find the appropriate QD arrays structures for achieving single-electron transfer operation with maximum yield, independent of parameter variations. We use for this purpose the term of "single-electron transfer success rate" defined as the ratio of successful configurations (i.e., configurations that exhibit single-electron transfer plateaus) to the total number of configurations investigated.

We find that the degree of non-uniformity in dot-gate capacitance (C_g) distribution within the arrays has a strong effect on single-electron transfer success rate for arrays containing four or more QDs. On the other hand, for 3QD systems the single-electron transfer success rate is not

affected by the degree of non-uniformity, allowing the identification of a most suitable QD structure for high-yield single-electron transfer operation. We draw guidelines for fabricating single-electron transfer devices with high yield based on our numerical findings.

2. Simulation Model and Calculation Method

Figure 1(a) shows the schematic structure of doped-nanowire FETs investigated for single-electron transfer.[19] These devices have been fabricated on silicon-on-insulator (SOI) (100) wafers with a buried oxide thickness of 400 nm. The final thickness and length of the nanowire channel is about 10 nm and 100 nm, respectively, while its width is smaller than 100 nm. The channel as well as the source and drain regions are doped with phosphorus to a concentration $N_d \approx 1\times10^{18}$ cm^{-3}. For this concentration, the average inter-dopant distance can be estimated as $(N_d)^{-1/3}$ to be around 10 nm. A single front gate is coupled to the entire channel through a thin silicon dioxide layer of about 10 nm. Ionized dopants present in the channel modulate its potential and single-electron transport takes place through an essentially 1D QD array, which is illustrated in Fig. 1(b) as a typical potential profile simulated for few dopants with Coulombic potentials randomly placed inside a 100 nm×10 nm Si channel.[17] We can observe that the potential landscape contains a high degree of inhomogeneity, as expected due to the discrete and uncontrolled distribution of dopants. In the dc current-voltage characteristics measured for these doped-nanowire FETs, we observed Coulomb oscillations with split-peak features which is an evidence of the fact that electron transport is governed by the Coulomb blockade effect through a multiple-QD array. From the periodicities of the current oscillations in the range of 50 mV~150 mV we can estimate an average dot-gate capacitance on the order of 1~3 aF. Under ac-gate operation with frequency f, some of these devices exhibit fine current

plateaus or inflections aligned around $\pm ef$ levels, indicating that dopant-induced QD arrays are favorable for single-electron transfer operation.

In our numerical study, we treat inhomogeneous QD arrays containing 3~6 dots between source and drain. The results can be applied to dopant-induced QD arrays as in our experimental study, but they can be also easily generalized to lithographically-defined QD arrays. Figure 1(c) illustrates an equivalent circuit considered in our simulation with a single gate coupled simultaneously to the entire array of QDs.

Structural non-uniformity was purposely introduced in the dot-gate capacitance distribution $\{C_g\}$ within the arrays. It should be noted that the gate capacitances basically correspond to the sizes of the dots. The degree of non-uniformity is described by the standard deviation of C_g (std(C_g)). According to approximated estimations of capacitance values based on our previous experimental conditions and device structures, in the first step of simulation, C_g values were intentionally scattered with an average gate capacitance (C_g^{av}) of 1.2 aF. On the other hand, tunnel junction capacitances (C_j) of 0.5 aF, which is smaller than the C_g^{av}, and resistances (R_j) of 0.1 MΩ were assumed to be uniform. In this simulation, however, the condition of $C_j > C_g$ was ignored, although the possibility of $C_j > C_g$ cannot be excluded and might be of significance in practical device operations. The effects of other parameter conditions have to be studied further.

Under the condition of $C_j < C_g$, we assumed uniform junction parameters for simplicity, because it is expected that the effect of $\{C_j\}$ distribution is less important than that of $\{C_g\}$ distribution on the energy conditions for electron transport. Some results will be described in the next section [Fig. 2(a)]. This is probably because tunnel junction parameters mainly affect tunneling times, i.e., tunnel conductance. As well as the result in Fig. 2(a), previous test

simulations (Fig. 2(c) in ref. 19) also indicate that C_j inhomogeneity has only a weak effect on single-electron transfer. Non-uniformity in $\{R_j\}$ distribution has basically no effect on the ac characteristics except for higher operation frequencies. For simulating the ac characteristics of these QD arrays, a two-level ac-gate voltage (typically between 0 mV and 100 mV) was applied with a frequency f=1 MHz to the single gate. It is worth mentioning that the period of the pulse (1 μs) is much larger than typical tunneling times through any junction in the system (~ps order), which ensures that the system is able to reach equilibrium (stable) conditions despite the stochastic nature of tunneling. These stable conditions are dependent only on the free energy of the entire system at the high and low gate voltage levels. All simulations were performed at T=0 K for clarifying the physical mechanism in the absence of thermally-activated events.

Regarding the calculation method, we used in our study of single-electron transfer a Monte Carlo (MC) simulation developed based on the Coulomb blockade orthodox theory.[1,2] According to this theory, forward and reverse tunneling rates of electrons across a specific junction are given by:

$$\Gamma^{\pm} = \frac{1}{e^2 R_j} \frac{\Delta F^{\pm}}{\left[1 - exp\left(-\frac{\Delta F^{\pm}}{k_B T}\right)\right]} , \quad (1)$$

where e is the elementary charge and $\Delta F^{\pm}$ is the change in system free energy due to forward or reverse tunneling events. The free energy is calculated as the sum of total electrostatic energy of the system and the work performed by external sources. The above equation simplifies for T=0 K in the following form:

$$\Gamma^{\pm} = \begin{cases} 0 & (\Delta F^{\pm} < 0) \\ \frac{\Delta F^{\pm}}{e^2 R_j} & (\Delta F^{\pm} > 0) \end{cases} , \quad (2)$$

As described also by Eq. (2), tunneling events are allowed only if they lower the free energy of the entire system. The average interval between successive tunneling events estimated from Eq.

(2) is $1/\Gamma^{\pm}$. We use in our simulation tunneling intervals $u^{\pm}$ that incorporate a random number r (0< r <1) in the calculation[20] in order to reflect the stochastic nature of the tunneling events, as shown in the following equation:

$$u^{\pm} = \frac{1}{\Gamma^{\pm}} ln\left(\frac{1}{r}\right) , \qquad (3)$$

For all tunnel junctions, we calculate $u^{\pm}$ values and choose a tunneling event with the minimum $u^{\pm}$, which is regarded as the tunneling event that actually occurred. We then repeat the same procedure for the next events starting at $t=u^{\pm}$.

We utilize this algorithm to simulate the source-drain current (I_{sd}) versus source-drain bias (V_{sd}) characteristics for ac-gate operation as described above. For each V_{sd} value the current is obtained from 1000 gate voltage cycles (i.e., measurement time is typically 1 ms). The criterion for achieving single-electron transfer operation consists of the occurrence of a plateau in these I_{sd}-V_{sd} characteristics perfectly aligned at ef current level. If this is observed, it means that a single electron is transferred from source to drain during each cycle of ac-gate voltage and the respective structure is considered a successful single-electron transfer device.

3. Results and Discussion

In non-uniform multiple-QD arrays, it should be expected that the arrangement of QDs inside the array plays a critical role in transport. Single-electron transfer operation especially should be even more sensitive to the QD arrangement. In order to emphasize this point, we pick up two examples of 4QD arrays which are identical in parameters (same C_g^{av} of 1.2 aF and same std(C_g) of about 0.4 aF), but different in dot arrangement between source and drain. Figures 2(a) and 2(b) show the equivalent circuits of these QD arrays and their simulated ac I_{sd}-V_{sd} characteristics (solid curves correspond to the circuits with uniform junction capacitances). The

dashed circles schematically indicate the arrangement of the dot-gate capacitances. For the array in Fig. 2(a), it is found that the I_{sd}-V_{sd} curves contain a plateau at ef current level which indicates that single-electron transfer was achieved. In other words, for V_{sd}=40 mV~50 mV electrons are transferred one by one every cycle of the ac-gate voltage (V_g) in a turnstile-like manner. On the other hand, the array in Fig. 2(b) does not exhibit a similar turnstile behavior when operated under the same conditions. The I_{sd}-V_{sd} characteristics corresponding to this case do not contain the ef plateau which defines single-electron transfer operation. This result clearly confirms that the QD arrangement can strongly modify the energy conditions inside the system affecting the processes necessary for single-electron transfer operation. When we consider dopant-induced QD arrays obtained by conventional doping, each device has basically its own QD array structure since dopant positions are not controlled. Therefore, at this stage of the study it is important to provide a statistical picture of the feasibility of single-electron transfer devices based on dopant-induced QD arrays.

The effect of $\{C_{\mathrm{j}}\}$ distribution is shown in Fig. 2(a), which contains the simulated I_{sd}-V_{sd} characteristics for a fixed $\{C_g\}$ arrangement, but a few different $\{C_j\}$ configurations. It can be observed that $\{C_j\}$ arrangement have only a small influence on the features of the electrical characteristics. The main point is that the single-electron plateau at I_{sd}=ef is maintained independent of $\{C_j\}$ arrangement, at least for relatively small or intermediate std(C_j). This suggests that the possibility of single-electron transfer is mainly governed by the distribution of $\{C_g\}$. We should note, however, that this result is obtained in case that C_{j}<C_g. Further study is needed for different parameter ranges.

We proceed to the statistical analysis as follows. We consider fixed values for average dot-gate capacitances (C_g^{av}), tunnel junctions (C_j, R_j), operation frequency (f) and levels of the

applied pulsed gate voltage (V_g^H and V_g^L) for all cases investigated. The value of std(C_g) is used as a parameter, being modified in the range of $0.1\times C_g^{av}\sim 0.75\times C_g^{av}$. For each given value of std(C_g), a set of N values is generated for C_g for systems with N QDs (N=3~6). Using these sets of $\{C_{g1}, C_{g2},\ldots, C_{gN}\}$ values, we form at random a statistical number ($\sim N^2$) of different QD arrangements. The ac characteristics were then simulated for each configuration in part, monitoring the occurrence (or absence) of *ef* plateaus.

Figure 3(a) shows the statistical results illustrating the effects of C_g dispersion on the success rate of single-electron transfer, defined as the ratio of the number of successful cases (i.e., cases that exhibit *ef* plateaus in the simulated I_{sd}-V_{sd} characteristics) to the total number of investigated cases. We discuss first the results obtained for QD arrays containing more than 4 dots. These longer arrays exhibit non-linear dependences of single-electron transfer success rate on std(C_g). It appears that initially, as the degree of non-uniformity is increased, the success rate for single-electron transfer operation increases as well from 15-25% to about 65-75% of the total number of cases investigated. For uniform or quasi-uniform arrays, it is difficult to achieve the conditions for single-electron transfer and the success rate is quite low. This may be due to the inability of these systems to trap an electron inside the array, which is one of the necessary conditions for achieving single-electron transfer. By enhancing the dot size non-uniformity (i.e., by increasing std(C_g)), electrons can become trapped more easily typically in one of the larger dots found inside the array. The “barriers” necessary for confinement can be formed due to the mismatch of dot-gate capacitances of neighboring dots. After std(C_g) becomes larger than some critical value (peak value), the success rate for single-electron transfer operation decreases and for some of our results (particularly, 6QD systems) the rate then exhibits an increasing tendency. According to our previous work, Fig. 3 in ref. 19, it is quite natural to assume that the success

rate has an oscillatory behavior with std(C_g). This can be related to the effect of discrete addition of charges into the system as the inhomogeneity is enhanced. In fact, we found that the number of such additional electrons that are injected into the system increases in steps with increasing std(C_g). These additional charges should effectively reshape the free energy profile of the entire system and effectively suppress the increasing inhomogeneity, in relationship with the periodicity induced by the addition of elementary charges. In other words, it is supposed that the actual increase in std(C_g) is compensated by the addition of charges into one of the dots in the system: With this charge addition, the respective dot can be considered as having a reduced C_g.

We statistically found that for systems with 4, 5, and 6 QDs the std(C_g) value corresponding to the maximum success is dependent on the number of dots in the system. Increasing the number of dots leads to a shift of the maximum success rate towards lower values of std(C_g). This result cannot be clarified at this point and it needs further study.

Our focus at this stage falls, however, on investigating the robustness against device parameter variations of single-electron transfer operation in nanometer-scale structures. From this point of view, the chance of realizing single-electron transfer in systems as discussed above (4~6QD arrays) seem to be strongly affected by variations of the degree of non-uniformity in {C_g} distribution. We could find only few particular QD array configurations stable against parameter fluctuations for some finite range of std(C_g). Therefore, it is practically impossible to identify QD arrays with more than four dots that can work as single-electron transfer devices even when parameter fluctuations are taken into account. As far as fabrication of single-electron transfer devices is concerned, restrictions imposed by such limited range of parameters available for single-electron transfer operation are undesirable.

The case of 3QD arrays is strikingly different from those of 4~6QD arrays. Single-electron transfer success rate is independent of the degree of non-uniformity in $\{C_g\}$ distribution for the entire range of parameters investigated. It appears that one third of the configurations considered here work as single-electron transfer devices. By analyzing the dot arrangements, the ideal single-electron transfer structures can be found as 3QD systems with a larger central dot. These structures always allow single-electron transfer operation. We performed an extended analysis of these 3QD arrays and we found that generally systems with gate capacitances of the outer dots smaller than that of the central dot are favorable for single-electron transfer. We will denote these arrangements from this point on as "S-L-S" structures due to their smaller-larger-smaller C_g arrangement ($C_{g1} \approx C_{g3} < C_{g2}$). The success rate of practically 100% for S-L-S arrays is illustrated in Fig. 3(b) together with a schematic equivalent circuit. This finding is promising for developing high-yield single-gated single-electron transfer devices since the S-L-S structures appear to be immune to parameter variations.

The transfer mechanisms that lead to the special behavior of 3QD arrays is described in Fig. 4 for two different cases, with the central dot having the largest and, respectively, smallest gate capacitance in the system. System free energy profiles have been calculated for this purpose as a function of the position of the transfer electron inside the array. For the S-L-S device with the central dot larger than the outer ones (shown in Fig. 4(a)), the I_{sd}-V_{sd} characteristics exhibit current plateau at *ef* levels (see Fig. 4(b)) and hence this single-gated QD array clearly operates as a single-electron transfer device. Free energy profiles are given in Fig. 4(c) in the order of the single-electron tunneling events. Free energy was calculated within the *ef* plateau region (for V_{sd}=45 mV) at the high level (V_g^H) and at the low level (V_g^L) of the pulse for different background charge configurations (indicated in brackets for each free energy profile). This

background charge (n_1 n_2 n_3) indicates the charge state, in which the system can be found at various times during the pulse period, with n_i being the number of electrons in the ith dot. Possible tunneling events are indicated by arrows and numbered in time sequence, while forbidden transfers are marked by crossed arrows. When gate voltage level is high (V_g^H), an electron is allowed to enter the larger central dot 2 from source following tunneling events 1 and 2 (see upper panel). After that, no other events are possible since all tunnel junctions are in the Coulomb blockade state during the high level of the pulse (V_g^H). When gate voltage level is changed to low (V_g^L), the electron residing on dot 2 remains initially trapped (as seen in the middle panel), but it becomes now possible for an electron to be removed from dot 3, leaving behind a hole (event 3 in the bottom panel) and altering consequently the free energy profile. Under these conditions (i.e., a favorable free energy profile for the (0 0 -1) charge state), the previously trapped electron can move to dot 3 and recombine with the existing hole (event 4), resetting the system to its (0 0 0) state. The transfer sequence is repeated again during the next pulse periods and thus one electron is effectively transferred from source to drain in every V_g cycle. Our preliminary studies show that this mechanism is essentially applicable for any S-L-S configurations, independently of the choice of C_g values, as long as the central dot capacitance is maintained larger than the outer ones.

The case shown in Fig. 4(d) for an L-S-L array with a smallest central dot is definitely different. As seen in Fig. 4(e), the I_{sd}-V_{sd} characteristics do not exhibit any single-electron transfer features. The reason for this failure can be understood from the free energy profiles shown in Fig. 4(f) calculated also for V_{sd}=45 mV (same value as for the previous case). At V_g^H, one electron can be injected from source into the large dot 1 (event 1 in the upper panel), but not further away into the array due to the Coulomb blockade, and then it returns to the source at V_g^L

(event 2 in the middle panel). No other events are allowed within the system (as indicated in the bottom panel) and hence single-electron transfer cannot be realized.

On the other hand, 4~6QD arrays with largest central (or near-central) dot do not exhibit such special behavior as in the SLS 3QD system. In these systems, charges can be trapped at various dots, which are not always the largest dot, resulting in often unsuccessful single-electron transfer. In fact, our statistical analysis did not reveal any configuration for 4-6QD arrays that can allow single-electron transfer with 100% success rate.

We can derive several conclusions from this statistical analysis: (a) single-gated inhomogeneous 1D QD arrays exhibit single-electron transfer features with a fairly high probability – this supports our frequent experimental observations of single-electron transfer in doped-nanowire FETs; (b) an optimal structure for single-electron transfer is a 3QD array with larger gate capacitance of central dot as compared with the outer ones (so-called “S-L-S” structure).

4. Guidelines for Fabricating High-Yield Single-Electron Transfer Devices

Identification of a suitable QD structure for single-electron transfer operation is encouraging for designing devices able to provide this ordered function even when natural parameter fluctuations must be taken into account. Several methods that we propose for fabricating single-gated single-electron transfer devices able to provide a maximized yield are depicted in Fig. 5.

One way to realize favorable S-L-S QD arrays is to utilize the potential fluctuations introduced by individual dopants. However, for this purpose we have to find a practical way to partly control the statistical distribution of dopants. One possible approach to accomplish this

goal is illustrated in Fig. 5(a). Selective doping of nanowires with a larger spatial extent allowed for doping of the central part as compared with the lateral regions can lead to the desired results. The outer QDs with smaller C_g can be formed ideally by a single dopant, while the central dot with larger C_g can be obtained due to superposition of the Coulombic potentials of two or few dopants confined by the fine patterning. For instance, assuming a controllable doping technique for a concentration N_d=1×10^{18} cm^{-3} and a Si channel width and thickness of 10 nm each, then the pattern for selective doping should be (10 nm, 20 nm~30 nm, 10 nm) in lengths to provide statistically a distribution of (1, 2~3, 1) dopants in the respective regions. S-L-S structures that can work effectively as single-electron transfer devices can be thus constructed based on the single-electron/single-dopant elementary unit.

A key point that has to be considered is the present development of single-atom doping techniques. There are basically two approaches in this direction using scanning tunneling microscope (STM) techniques and conventional ion implantation techniques with focused beams. In the first approach, single dopants can be precisely placed in the Si lattice to about 1nm accuracy.[21] It is necessary, however, to develop techniques to integrate these processes with standard Si technology. Some important steps have been already taken in this direction.[22] On the other hand, techniques based on low-energy single-ion implantation have at present aiming precisions of about 60 nm.[23] This resolution is expected to be improved in the future, but seems to be still too low for designing the ideal single-electron transfer devices based on single dopants. Therefore, it is necessary to develop present techniques and/or to find alternative methods for single dopant implantation control which could satisfy the requirements envisaged in this paper.

Finally, we point out again that our findings can be extended also to lithographically-defined QD arrays. As illustrated in Fig. 5(b), the desired S-L-S arrays can be

simply realized by purposely designing a larger central dot. In this direction, it is important to minimize the sizes of the tunnel junctions and of the dots for achieving single-electron transfer capabilities. This approach can be promising for room temperature operation of single-gated single-electron transfer devices based on the structural conditions that we described in this paper.

Lithography techniques facilitate rough controllability of the QD sizes, but it is still difficult to precisely suppress size fluctuations. In this work, we demonstrated that 3QD arrays with larger central dot possess high robustness against parameter fluctuations and this can be useful in solving the above problem. Further experimental studies along both the above-mentioned directions are currently carried out.

5. Summary

We performed a statistical study on the effects of parameter variability on single-electron transfer operation for single-gated inhomogeneous 1D arrays of QDs. This study was focused on providing theoretical evidence for the frequent observation of single-electron transfer in doped-nanowire FETs, in which random dopant potentials create arrays of naturally inhomogeneous QD-like structures. We found that non-uniformity strongly affects the yield of devices comprising more than 4QDs. On the contrary, devices with 3QDs exhibit a special behavior, allowing us to distinguish ideal structural conditions for single-electron transfer operation and to propose several designs for the reproducible fabrication of future single-electron transfer devices.

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Figure Captions

Fig. 1. (Color online) (a) Device structure of a single gate doped-channel FET fabricated on SOI substrate. (b) Potential landscape due to the presence of few (in this example, four) phosphorus ions in a section of 100 nm×10 nm of the channel. (c) Schematic equivalent circuit for theoretically describing inhomogeneous QD arrays.

Fig. 2. (Color online) (a) and (b) Equivalent circuits and simulated I_{sd}-V_{sd} characteristics for different arrangements of QDs in two 4 dots systems with the same average gate capacitance of 1.2 aF and standard deviation of ≈0.4 aF. In (a) single-electron transfer occurs as plateaus at *ef* current levels. The solid curve corresponds to uniform junction capacitances, while the dashed curves were simulated for various non-uniform arrangements of $\{C_j\}$. In (b) *ef* plateaus cannot be observed.

Fig. 3. (Color online) (a) Success rate of single-electron transfer cases (defined as ratio of cases exhibiting *ef* plateaus in the simulated I_{sd}-V_{sd} characteristics to total number of cases investigated) for 3, 4, 5, and 6 dots systems and (b) success rate of 3QD cases with a larger (L) dot at the center and smaller (S) dots at the ends of the array, i.e., S-L-S arrays (as shown in the inset).

Fig. 4. (Color online) (a) Equivalent circuit, (b) simulated ac I_{sd}-V_{sd} characteristic and (c) free energy profiles calculated at V_{sd}=45 mV and different levels of V_g for a case with larger central dot (C_{g1}=1.2 aF, C_{g2}=1.6 aF, and C_{g3}=0.8 aF). Single-electron transfer operation can be achieved in this situation, seen as a current plateau at *ef*. The transfer mechanism is explained in time sequence by the panels in Fig. 4(c). (n_1 n_2 n_3) indicate background charge configurations for each free energy profile, where n_i is the number of electron in the *i*th dot. Possible tunneling events are indicated by arrows and numbered in time sequence, while forbidden transfers are marked by

crossed arrows. (d)-(f) Same plots for a case with small central dot (C_{g1}=1.6 aF, C_{g2}=0.8 aF, and C_{g3}=1.2 aF). For this situation, single-electron transfer cannot be realized (no *ef* plateaus can be observed) which is explained by the analysis of the free energy profiles in Fig. 4 (f).

Fig. 5. (Color online) (a) Possible discrete few-dopant distribution after selective doping of the nanowire and contour plot of dopant-modulated potential illustrating the formation of an S-L-S-like structure, i.e., a 3QD arrays with the gate capacitances arranged as $C_{g1} \approx C_{g3} < C_{g2}$. (b) Lithographically-defined 3QD array with purposely-designed S-L-S structure for single-electron transfer.

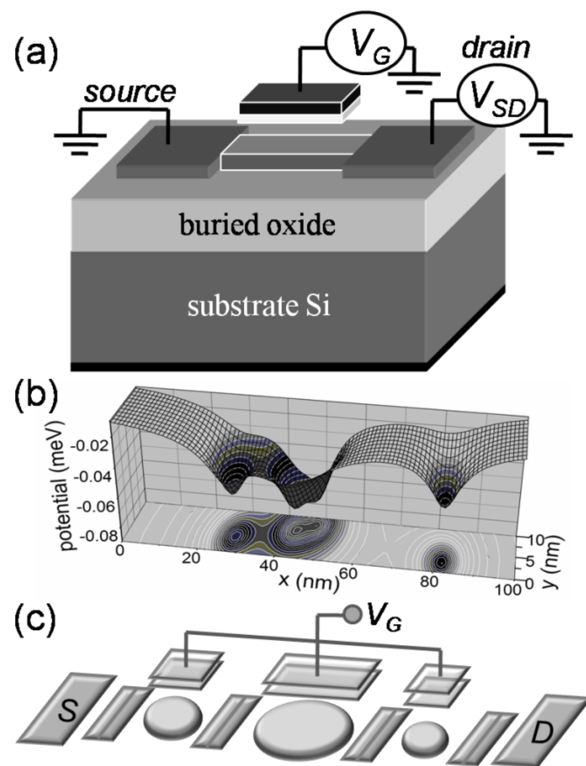

Fig. 1. K. Yokoi *et al*., Jpn. J. Appl. Phys.

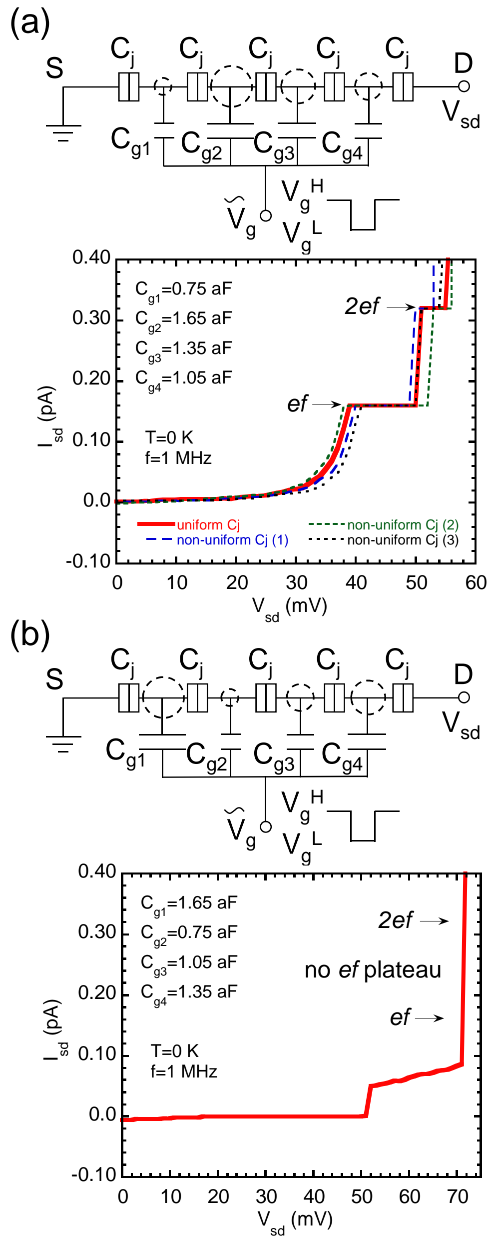

Fig. 2. K. Yokoi *et al.*, Jpn. J. Appl. Phys.

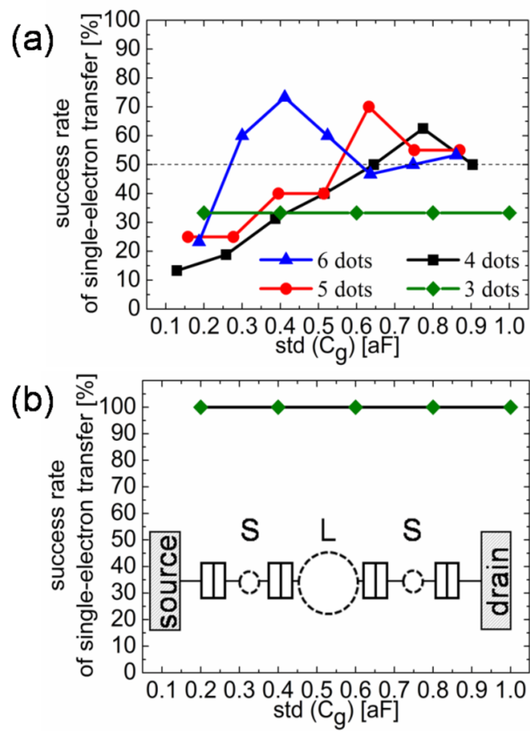

Fig. 3. K. Yokoi *et al*., Jpn. J. Appl. Phys.

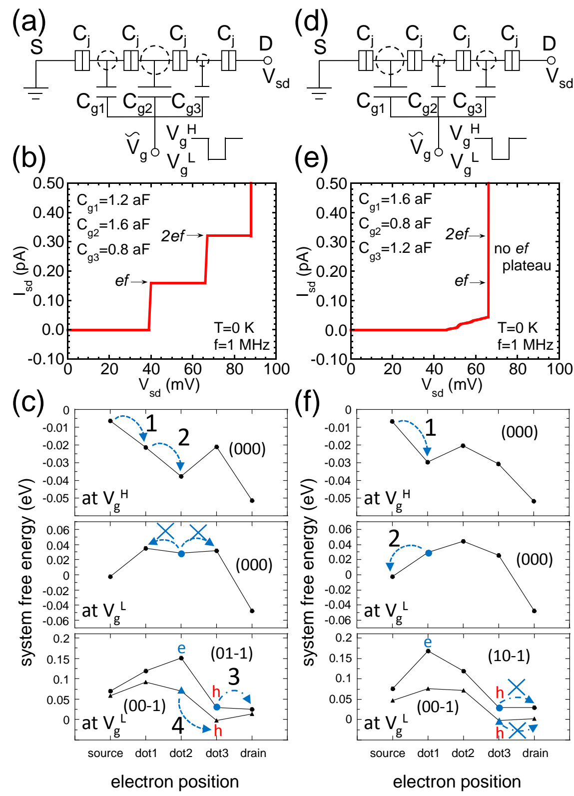

Fig. 4. K. Yokoi *et al.*, Jpn. J. Appl. Phys.

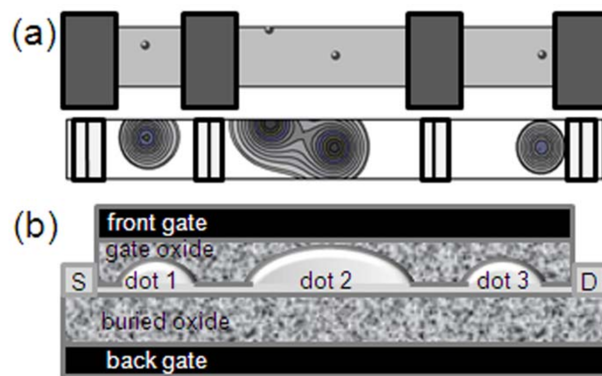

Fig. 5. K. Yokoi *et al*., Jpn. J. Appl. Phys.