Observation of Discrete Dopant Potential and Its Application to Si Single-Electron Devices

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Abstract

Single-electron devices are attractive because of their ultimate capabilities such as single-electron transfer, single-electron memory, single-photon detection and high sensitivity to elemental amount of charge. We studied single-electron transport in doped nanoscale-channel field-effect transistors in which the channel potential is modulated by ionized dopants. These devices work as arrays of quantum dots with dimensions below present lithography limits. We demonstrate the ability of dopant-induced quantum dot arrays to mediate the transfer of individual electrons one at a time (single-electron transfer). We also monitored the actual dopant distribution and observed single dopant potentials using low temperature Kelvin probe force microscopy.

Keywords: single-electron transfer, quantum dots, single dopant potential, silicon-on-insulator, Kelvin probe force microscope.

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Introduction

Single-electron devices (SEDs) are attractive candidates for future electronics due to their ultimate capabilities of controlling elementary charge transport and due to their ultrahigh sensitivity [1]. Applications such as single-electron transfer [2-4], single-electron memories [5], single-photon detection [6], and detection of single dopant ionization [7] have been already proposed and demonstrated in devices containing quantum dots (QDs). Reducing the size of the QDs to nanometer scale is expected to improve the capabilities of SEDs from the viewpoints of operation temperature and speed. However, this reduction is strongly relying on progress in nanolithography techniques.

Different from the above-mentioned approach, we have recently investigated the properties of doped-nanowire field-effect transistors (FETs) in which QD arrays are formed by the superposition of individual dopant potentials. We have demonstrated the capabilities of these structures to realize single-electron transfer operation, i.e., to mediate the time-correlated transfer of single electrons under the application of gate pulses [8]. We have also found by extensive simulations that single-electron transfer ability is enhanced for three-QD systems, particularly when the central dot is larger [9]. These results provide important insights for future design optimization of single-electron transfer devices utilizing dopant potentials. Monitoring the discrete dopant distribution at nanoscale is an important component of such designs. We have utilized a technique based on low-temperature Kelvin probe force microscopy to detect individual dopant potential in nanoscale devices even under operating conditions [10]. In this paper, we are describing these recent findings focusing on the importance of the interplay between single electrons and individual dopant atoms.

Dopant-induced quantum dot arrays

Dopants have been an essential component of electronic devices playing the role of extrinsic charge providers for transport. They are also used to create the p-n junctions necessary inside the FETs – the basic building block of the electronic industry. However, as FET channel dimensions are brought down to only few tens of nanometers, the number of dopants in the channel is strongly reduced and their discrete distribution starts to play a significant role in device operation [11]. On the other hand, this discreteness brings attractive applications based on the interplay between the potential modulation induced by individual dopants and single charges [12]. Recently, transport spectroscopy studies of single-phosphorus FETs [13] and single-boron FETs [14] have been performed, revealing the discrete character of this interaction.

Figure 1(a) illustrates the effect of a single donor dopant on the potential of a silicon nanowire. The ionized dopant introduces a Coulombic potential well with a spatial extension on the order of several nm and a potential depth of several tens of mV [15]. In this well, a single electron can be confined which effectively neutralizes the dopant atom and implicitly flattens the potential landscape. The dopant-induced potential dip works thus effectively as a QD. In nanostructures containing a larger number of dopants, for instance as shown in Fig. 1(b) for channels of $100\times50\times10\ nm^3$ with a doping concentration $N_d=1\times10^{18}\ cm^{-3}$, the potential landscape becomes more complex and the channel generally works as a multiple-QD array. In these arrays transport occurs also by single-electron tunneling through the dopant-induced QDs [16]. The advantage of this multiple-QD structure is that it is more suitable for applications towards controlled transfer of charges. This is why we are focusing on investigating the properties of doped one-dimensional nanowire FETs under electric fields.

Single-electron transfer in doped-nanowire FETs

Single-electron transfer [2,3], i.e., shuttling of only one electron between source and drain electrodes every cycle of ac gate voltages, is one of the key issues for future electronics. This would open the path to utilizing individual electrons for conveying one bit of information in logic or memory circuits. Another application of interest is developing a current metrological standard which is currently not a stand-alone one [17]. Realizing this ordered function based on the electron-dopant interplay in silicon is essential in the frame of the above-mentioned applications.

We studied nanoscale FETs, as shown in Fig. 2(a), made on silicon-on-insulator (SOI) substrates and having the channel moderately doped same type as source and drain pads (n-type for this study). Typical dimensions of the channel are 100 nm in length, and 10 nm in width and height, while the channel doping concentration was estimated to be $N_d \approx 1\times10^{18}$ cm^{-3}. The potential profile is expected to be similar to the one shown in Fig. 2(b), simulated for 10 dopants as estimated to be present in the channel. A single front gate is coupled to this channel through a gate oxide layer about 50 nm thick. Figure 2(c) shows the dc I_{sd}-V_{fg} characteristics measured at 5.5 K for a source-drain bias V_{sd}=10 mV. Sharp current oscillations can be observed with an irregular pattern which indicates the formation of a multiple-tunnel-junctions (MTJ) array in the device channel. Undoped FETs with comparable dimensions do not exhibit such sharp and irregular oscillations which supports the conclusion that the MTJ array is originated from the ionized dopant impurities.

The dc I_{sd}-V_{sd} characteristics (dashed curve in Fig. 2(d)) contain a wide zero-current region around V_{sd}=0 V. This confirms that transport is prohibited for small biases according to the Coulomb blockade physics [18]. However, when an ac gate voltage is applied to the front

gate, the potential in the channel is shifted up and down periodically. This way, electrons are trapped inside the dopant-induced QD array during the high level of the pulse and removed during its low level application. Figure 2(d) shows ac I_{sd}-V_{sd} characteristics (solid curve) measured at 5.5 K for an ac frequency of 1 MHz. The inflections (small plateaus) marked in the figure correspond to current level $I_{sd}=\pm e\times f$ (where e is the elementary charge). This means that the current is composed of one electron transferred between source and drain during each cycle of the ac gate voltage. This is a clear signature of single-electron transfer and in these devices this ordered transfer operation is achieved in non-uniform QD arrays naturally formed by dopants. This finding is promising for developing functional single-electron transfer devices based on dopant-induced QD arrays [8].

An essential point to be addressed is the non-uniformity in dopant distribution associated with the conventional doping techniques. We addressed this issue by simulations of the effects of parameter dispersion on the single-electron transfer characteristics. As a first step, we studied the effect of dot size (gate capacitance) dispersion utilizing a Monte Carlo simulation technique [19] based on the orthodox theory of Coulomb blockade [18]. A statistical number of systems with 3-6 QDs serially arranged in one-dimensional arrays and coupled to a common gate have been investigated under ac gate operation using the standard deviation of the gate capacitance distribution (std(C_g)) as a parameter [9]. We focused on the occurrence probability of single-electron transfer and we used for this purpose the term of "single-electron transfer success rate", defined as the ratio of successful configurations (i.e., configurations that exhibit single-electron transfer plateaus) to the total number of configurations investigated.

The statistical results for one-dimensional arrays with 3-6 QDs are shown in Fig. 3(a). The single-electron transfer chance is generally enhanced in QD arrays with higher std(C_g) (i.e.,

higher QD size dispersion). Most importantly, however, we found that for arrays of 3 QDs we can precisely identify optimal structures that will invariably exhibit single-electron transfer features with high robustness. These favorable structures, shown schematically in Fig. 3(b), contain a central QD larger than those next to source and drain (so-called S-L-S array due to the small-large-small arrangement of the QD sizes). This provides us guidelines for fabricating operational single-electron transfer devices by combining the random distribution of dopants with geometrical control over the dopant-induced QD array. Such a proposal is shown in the upper part of Fig. 3(c), in which the design of the Si channel allows a larger number of dopants to be statistically found in the central part of the channel. This is expected to enhance the probability of creating a larger dopant-induced QD there by the superposition of individual dopant potentials. As nanolithography techniques advances, it may be also possible to realize S-L-S structures with lithographically-defined QD (as illustrated in the lower part of Fig. 3(c)) with dimensions comparable to their dopant-based counterparts.

Direct observation of individual dopant potentials by low temperature KFM

Monitoring the dopant distribution in nanoscale channels is of paramount importance considering the fact that at these small dimensions the discreteness of the dopants plays a significant role on determining the device parameters. Several methods are available for shallow dopant profiling or carrier concentration evaluation, such as scanning tunneling microscopy (STM) [20] or scanning capacitance microscopy (SCM) [21]. These methods have, however, some important drawbacks: STM can only provide information about few top-most layers, while SCM techniques do not offer sufficient resolution for detecting single dopants. Kelvin probe force microscopy (KFM) on the other hand seems to be an appropriate tool for investigating

dopant potential because of its higher resolution and sensitivity to charges placed deeper in the structure of the device [22].

Conventional KFM techniques are typically used at room temperature and as a consequence they have few serious drawbacks in detecting bare dopant potentials. This is because at room temperature free carriers accumulated in the device Si channel screen the fine dopant-induced potential fluctuations. In order to overcome this problem, we proposed a technique that utilizes the capabilities of the KFM at low temperature (13 K). Furthermore, our low temperature (LT)-KFM allows biasing of the device during measurement, so the potential in the channel can also be controlled by means of external gates. Therefore, this LT-KFM system is a very promising tool for single dopant profiling.

Figure 4 shows line profile taken over the Si channel and the adjacent buried oxide (BOX) area for different values of the back gate voltage (V_g) at room temperature (300 K) in Fig. 4(a) and at low temperature (13 K) in Fig. 4(b). It can be noticed that surface potential over the BOX (right side) is changing with V_g similarly for both high and low temperatures. This is due to the fact that far from the channel the BOX layer is floating, reflecting thus the potential of the underneath p^+-Si substrate (used as back gate). The difference of about -2 V from the expected values may be ascribed to surface charges on the BOX layer that cannot be modified by V_g due to the large thickness of the BOX (about 150 nm). The potential over the channel (left side), on the other hand, behaves completely different at high and low temperatures. In the room temperature measurement, channel potential is pinned at around 1 V independent of V_g. At 13 K, the channel surface potential is strongly dependent on V_g, which indicates that the thin Si layer behaves almost as an insulator. We suggest that this behavior is due to the freeze-out effect of dopants in the channel. While at room temperature the channel is conductive so that its potential

remains pinned close to the ground level, at low temperature the number of ionized dopants (and implicitly free carriers) is strongly reduced and the channel becomes partially floating. As a consequence, its surface potential can be modulated by applying V_g from -4 V to +4 V. The occurrence of the freeze-out effect can be deduced also by plotting the potential difference observed when applying V_g of -4 V and +4 V as a function of temperature (measurements were performed at 13K, 38 K, 70 K, and 300 K). These results already indicate the strong ability of KFM operated at low temperatures to overcome the problem of the screening free carriers. In fact, fine potential fluctuations become observable in the channel even in these results, as will be shown in more detail in the following.

Figure 5(a) shows the expected surface potential map simulated for a nanoscale Si channel with $N_d=1\times10^{18}$ cm^{-3}. Phosphorus dopants have been randomly placed inside this nanowire mesh and the potential resulting from the superposition of all individual Coulombic potentials was calculated. The non-uniform potential landscape is related to the non-uniform dopant distribution. However, potential dips coming mainly from individual dopants can be extracted even from this complex profile, as shown in Fig. 5(b).

The surface potential measured using LT-KFM on a phosphorus-doped thin-layer FET channel is shown next in Fig. 6(a). For these devices, doping concentration was estimated to be around 1×10^{18} cm^{-3} which means that the average inter-dopant distance is about 10 nm. The substrate Si (p-type) was used as a back gate. The image in Fig. 6(a) was taken for V_g=-3 V when we consider that the channel is depleted of free carriers and the potential modulation due to the bare ionized dopants can be more visible. In order to confirm that the fine potential fluctuations noticeable in this image come mainly from individual dopants, line profiles taken at different locations are shown in Figs. 6(b) and (c). The lateral extension of 5-10 nm and the well

depth of 15-25 mV are consistent with the expected values for phosphorus in silicon (Bohr diameter of about 6 nm and depth of the dopant levels relative to Si conduction band of about 40 mV [13]).

As mentioned above, an important advantage of our KFM is the ability to control the free carriers in the channel with external biases and to measure the surface potential for devices under effectively normal operation. Figures 7(a)-(d) show surface potential maps measured for positively increasing values of the gate voltage V_g (-3, -2, -1, and 0 V, respectively). It can be seen that for more positive V_g, potential landscape becomes smoother and dopant-induced potential fluctuations are smeared out. This is due to the fact that more positive V_g lowers the channel potential compared to the source Fermi level allowing electrons to enter the channel and thus screen the dopant potentials. These results prove that LT-KFM may become an essential tool for correlating the transport characteristics and the actual dopant distribution in nanoscale SEDs.

Isolated single-atom detection is another attractive study direction which may give important insights into the physics of the pure interaction between single charges and single dopants. We have measured for this purpose thin-top-Si SOI sample with top layer only weakly doped with boron ($N_a \approx 1\times10^{16}$ cm^{-3}, i.e., an average inter-dopant distance of 40~50 nm). The surface potential map taken at 13 K is shown in Fig. 8(a). In this image two higher potential regions (also shown as line profiles in Fig. 8(b)) are expected to correspond to two ionized boron atoms. When holes are not present at the boron dopant site, the potential is lifted up compared to the neutral-boron state and to the surrounding undoped Si area. The specific features of these potential hills are also in good agreement with the estimations for boron in silicon. Due to such

findings, it is attractive to consider LT-KFM as a unique tool for observing discrete charging during single-electron transport in dopant-induced QD arrays [10].

Summary

At present Si nanodevices are evolving toward single atom sizes. For single-electron applications, an attractive direction of research concerns transport properties of individual dopant potentials. This may lead to a new era for electronic devices, completely different from classical devices that utilize statistical and continuous nature of matter due to the huge number of dopants involved in the operation. For future Si nanodevices, discreteness of both transferred and fixed charges will play a tremendous role in developing novel applications. We have demonstrated single-electron transfer operation using dopant-induced QD array and we have observed the channel potential modulated by discrete dopants using low-temperature Kelvin probe force microscopy.

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References

[1] D. V. Averin and K. K. Likharev, in *Single charge tunneling*, ed. H. Grabert and M. Devoret (Plenum, New York, 1992), p. 311.

[2] L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. **64** (1990) 2691.

[3] H. Pothier, P. Lafarge, P. F. Orfila, C. Urbina, D. Esteve, and M. H. Devoret, Physica B **169** (1991) 573.

[4] Y. Ono, A. Fujiwara, K. Nishiguchi, H. Inokawa, and Y. Takahashi, J. Appl. Phys. **97** (2005) 031101 and references therein.

[5] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and L. Seki, IEEE Trans. on Electron Dev. **41** (1994) 1628.

[6] R. Nuryadi, Y. Ishikawa, and M. Tabe, Phys. Rev. B **73** (2006) 045310.

[7] Z. A. Burhanudin, R. Nuryadi, and M. Tabe, Appl. Phys. Lett. **91** (2007) 042103.

[8] D. Moraru, Y. Ono, H. Inokawa, and M. Tabe, Phys. Rev. B **76** (2007) 075332.

[9] K. Yokoi, D. Moraru, M. Ligowski, and M. Tabe, Jpn. J. Appl. Phys. **48** (2009) 024503.

[10] M. Ligowski, D. Moraru, M. Anwar, T. Mizuno, R. Jablonski, and M. Tabe, Appl. Phys. Lett. **93** (2008) 142101.

[11] S. Roy and A. Asenov, Science **309** (2005) 388.

[12] B. E. Kane, Nature (London) **393** (1998) 133.

[13] H. Sellier, G. P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, and S. Biesemans, Phys. Rev. Lett. **97** (2006) 206805.

[14] Y. Ono, K. Nishiguchi, A. Fujiwara, H. Yamaguchi, H. Inokawa, and Y. Takahashi, Appl. Phys. Lett. **90** (2007) 102106.

[15] G. Evans, H. Mizuta, H. Ahmed, Jpn. J. of Appl. Phys. **40** (2001) 5837.

[16] T. Koester, F. Goldschmidtboeing, B. Hadam, J. Stein, S. Altmeyer, B. Spangenberg, H. Kurz, R. Neumann, K. Bruner, and G. Abstreiter, Jpn. J. Appl. Phys., Part 1 **38** (1999) 465.

[17] X. Jehl, M. W. Keller, R. L. Kautz, J. Aumentado, and J. M. Martinis, Phys. Rev. B **67** (2003) 165331 and references therein.

[18] K. K. Likharev, IEEE Trans. Magn. **23**, 1142 (1987).

[19] H. Ikeda and M. Tabe, J. Appl. Phys. **99** (2006) 073705 and references therein.

[20] M. Nishizawa, L. Bolotov, T. Kanayama, Appl. Phys. Let., **90**, 122118 (2007).

[21] W. Goragot, M. Takai , Jpn. J. Appl. Phys. **43**, 3990 (2004).

[22] M. Nonnenmacher, M. P. O'Boyle, and H. K. Wickramasinghe, Appl. Phys. Lett. **58** (1991) 2921.

Figure captions

FIG. 1. Surface potential profiles simulated for phosphorus-doped Si nanowires (as shown in the insets) containing: (a) one dopant and (b) 20 dopants.

FIG. 2. (a) Schematic structure of doped-nanowire FETs made on SOI substrates. (b) Simulated potential landscape for $N_d=1\times10^{18}$ cm^{-3} and channel dimensions comparable to real device (width and height of 10 nm and length of 100 nm). (c) dc I_{sd}-V_{fg} characteristics measured at 5.5 K for a doped-nanowire FET. (d) dc (dashed curve) and ac (solid curve) I_{sd}-V_{sd} characteristics at 5.5 K. Ac frequency of the front gate voltage pulse is 1 MHz. The current inflections marked occur at $I_{sd}\approx\pm e\times f$ indicating single-electron transfer.

FIG. 3. (a) Statistical effect of QD size dispersion (std(C_g)) on the success rate of single-electron transfer (proportion of cases exhibiting single-electron transfer out of the total number of cases investigated) for systems with 3~6 QDs. (b) Equivalent circuit of most favorable structure for single-electron transfer (S-L-S array, i.e., 3 QD array with small-large-small dot size arrangement). (c) Proposed methods for designing robust single-electron transfer devices based on selective doping or lithographically-defined QDs.

FIG. 4. (a)-(b) Surface topography (dashed curve) and surface potential line profiles (marked curves) taken by KFM over the Si channel and the adjacent oxide layer for different values of back gate voltage V_g (from -4 V to +4 V). Temperature was 300 K in (a) and 13 K in (b). (c) Dependence of the potential difference induced in the channel surface potential by application of V_g of +4 V and -4 V as a function of temperature.

FIG. 5. (a) Surface potential image simulated for $N_d=1\times10^{18}$ cm^{-3} obtained by superposition of randomly-distributes phosphorus atoms with Coulombic individual potentials. (b) Line profiles through two dopant-induced potential valleys.

FIG. 6. (a) Surface potential map of a phosphorus-doped FET channel obtained by KFM at 13 K. (b)-(c) Line profiles of local potential dips introduced by individual phosphorus atoms (taken in the marked areas in (a)).

FIG. 7. Surface potential maps of phosphorus-doped nanowire taken for different values of the back gate voltage V_g: (a) -3 V, (b) -2 V, (c) -1 V, and (d) 0 V, respectively.

FIG. 8. (a) Surface potential map of a boron-doped thin SOI layer obtained by KFM at 13 K. (b) Line profiles of local potential dips introduced by individual boron atoms (taken in the marked areas in (a)).

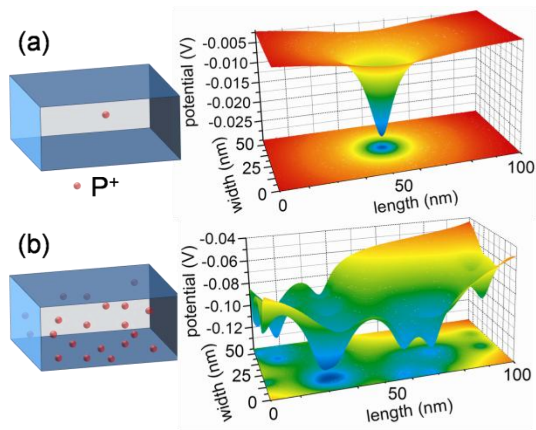


FIG. 1. Tabe *et al*., Thin Solid Films 2009

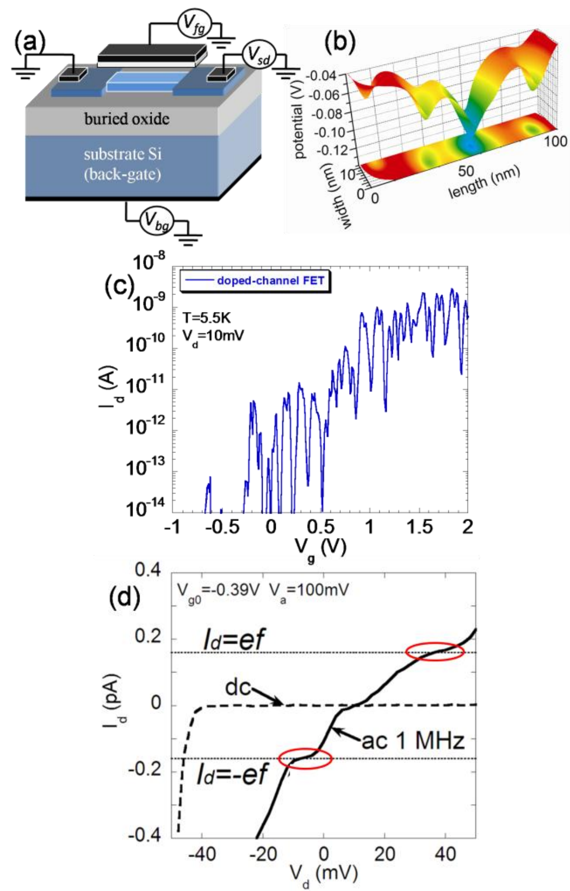
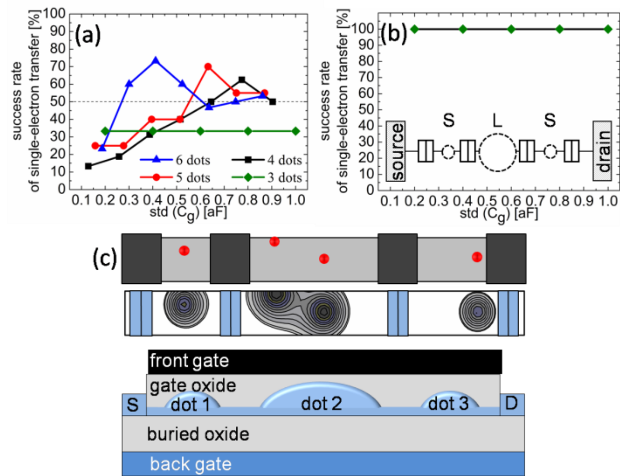


FIG. 2. Tabe *et al*., Thin Solid Films 2009



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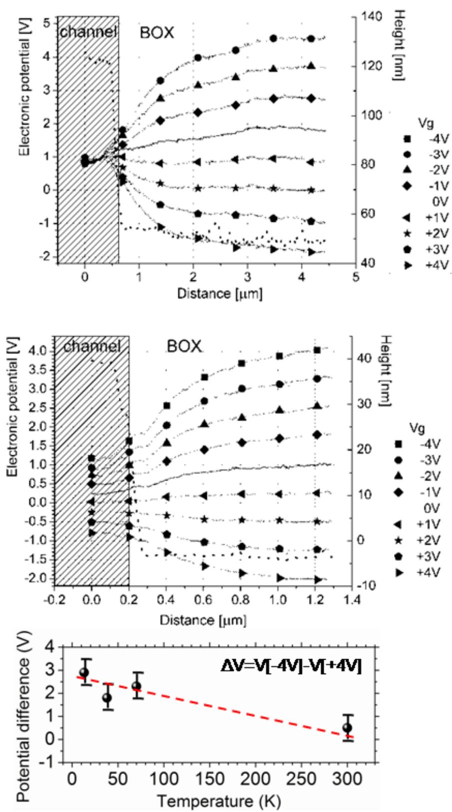

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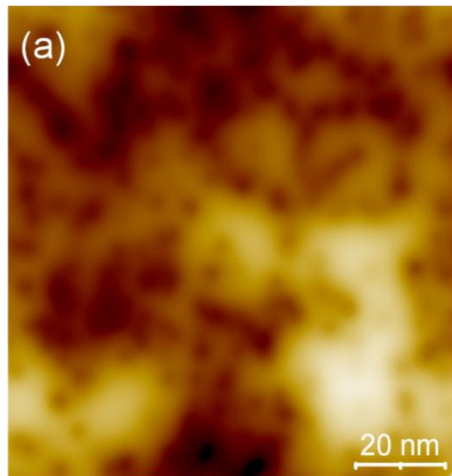

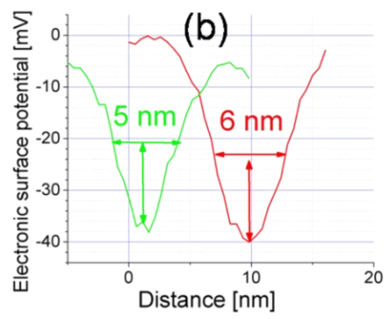

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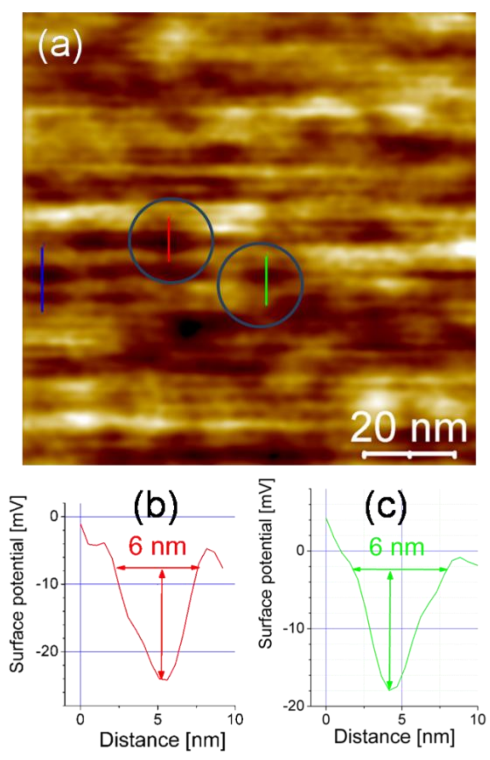
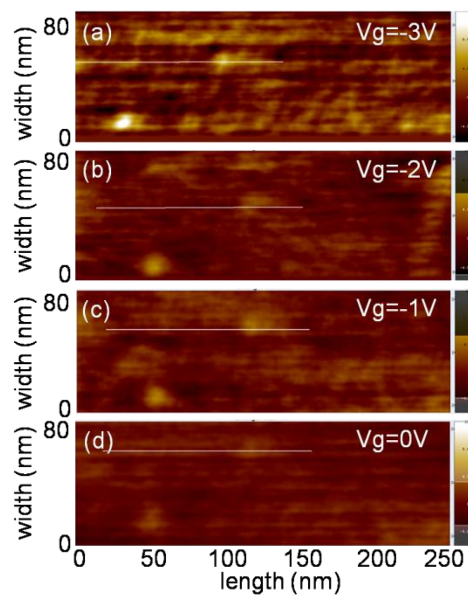


FIG. 6. Tabe *et al*., Thin Solid Films 2009



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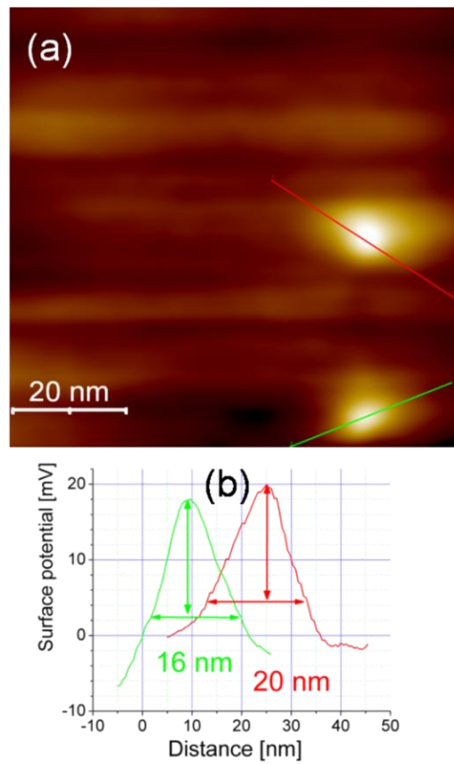

FIG. 8. Tabe *et al*., Thin Solid Films 2009