Electrical control of capacitance dispersion for single-electron turnstile operation in common-gated junction arrays

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We have studied single-electron turnstile operation in common-gated one-dimensional arrays of four tunnel junctions (three dots) having inhomogeneous junction capacitances. Analytical calculations show that the source-drain voltage range with a current plateau due to single-electron turnstile operation is increased when the outer two tunnel capacitances are adjusted to be smaller than the inner ones. In fact, we have demonstrated in phosphorous-doped silicon-on-insulator field-effect transistors (FETs) that back-gate voltage works to assist the turnstile operation, which is primarily ascribed to electrical control of junction capacitance dispersion, i.e., reduction in outer junction capacitances. As a result, postfabrication control of capacitance dispersion in multijunction FETs can be achieved, resulting in successful turnstile operation. © *2010 American Institute of Physics*. [doi:10.1063/1.3476305]

I. INTRODUCTION

Single-electron devices (SEDs) (Ref. 1) have generated great interest as candidates for future nanoelectronics because of their small sizes, low power consumption, and ability to manipulate elementary charges. One of the applications of SEDs is single-electron transfer, i.e., controllable transfer of electrons one-by-one synchronized with alternating external gate voltages. The basic design for single-electron transfer is a single-electron turnstile,[2] consisting of three serially-connected metallic islands and a gate coupled only to the central island. When an alternating voltage is applied to the gate, one electron can be transferred between the source and the drain during every voltage pulse. Single-electron transfer can also be realized in more complex designs, such as pumps[3,4] or ratchets,[5] in which two or more phase-shifted alternating gate voltages are used. Even a single-gate design in the turnstile, however, may be difficult in fabrication with the requirement of precise alignment between the gate and the central dot in nanometer scale.

This restriction can be relaxed if the gate is allowed to be coupled commonly to the entire array of dots, as schematically shown in Fig. 1(a). All quantum dots are coupled to the same gate through nontunnel capacitors, while they are coupled to each other through tunnel capacitors. Recently, single-electron turnstile in such common-gated dot arrays having homogeneous or inhomogeneous capacitances has been demonstrated theoretically[6–8] and experimentally.[9,10] In these papers, effect of dispersion of C_g, reflecting size variation in quantum dots, was primarily examined under assumption of uniform tunnel junction capacitances C_j for simplicity. It is undoubted, however, that C_j's also affect the Coulomb blockade conditions required for single-electron turnstile operation. Furthermore, it is expected that C_j dispersion may be partially controlled by a combination of two or more separated gates, although C_g dispersion appears to be almost determined by fabrication of the device, i.e., by the size of each dot.

In this paper, we study the effect of tunnel junction capacitance dispersion on single-electron turnstile operation and postfabrication controllability of the capacitance dispersion by using front- and back gates. We first perform an analytical study of the charge stability diagrams for three-dot arrays with a common gate and clarify the effect of inhomogeneity of the tunnel junction capacitances as well as gate capacitances on single-electron turnstile operation. Based on the analytical results, we then demonstrate experimentally controllability of the tunnel junction capacitances in doped-nanoscale silicon-on-insulator (SOI) field-effect transistors (FETs) for achieving single-electron turnstile.

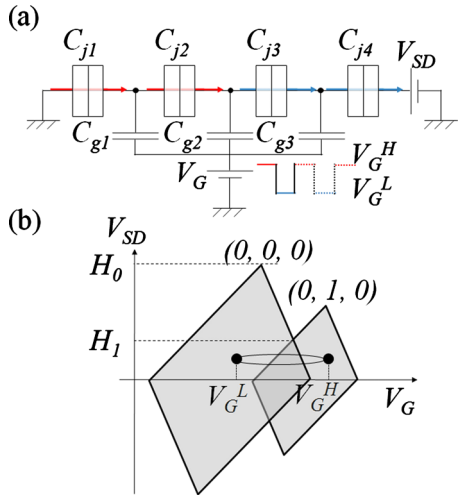

FIG. 1. (Color online) (a) Equivalent circuit for a three-dot array. The events that lead to single-electron turnstile are illustrated for the high voltage level V_G^H (red arrows) and for the low voltage level V_G^L (blue arrows). (b) Schematic charge stability diagram showing the (0, 0, 0) and (0, 1, 0) states in gate voltage (V_G)/source-drain bias (V_{SD}) plane, where the set (n_1,n_2,n_3) describes the number of excess electrons in each dot. The overlap of (0, 0, 0) and (0, 1, 0) domains has a V_{SD} extension H_1 and the (0, 0, 0) domain has a V_{SD} extension H_0 (used as a normalization factor).

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II. ANALYTICAL STUDY OF CAPACITANCE DISPERSION EFFECTS

We study arrays of three serially connected dots, as shown in the equivalent circuit of Fig. 1(a). Each dot is coupled to a common gate through gate capacitances C_{g1}, C_{g2}, and C_{g3}. Dots are coupled to each other and to electron reservoirs (source and drain) by tunnel junctions. These tunnel junctions are characterized by capacitances C_{j1}, C_{j2}, C_{j3}, and C_{j4}. Under Coulomb blockade conditions, certain charge states of the dots are stable and described by a set of excess electrons in each dot, (n_1,n_2,n_3).[11] Figure 1(b) schematically shows the voltage domains associated with (0, 0, 0) and (0, 1, 0) charge states in the gate voltage (V_G)/source-drain bias (V_{SD}) plane. The overlap between these two stable charge domains is a necessary condition for single-electron turnstile and, for the dot arrays considered in this paper, it is also a sufficient condition. When this condition is met, an alternating gate voltage can be set with its high level (V_G^H) to be in the (0, 1, 0) domain and its low level (V_G^L) to be in the (0, 0, 0) domain, as indicated in Fig. 1(b). Single-electron turnstile can be generally achieved according to the following sequence.[7] When the gate voltage is switched to the high level from the low level, the charge state also changes from (0, 0, 0) to (0, 1, 0). In this process, one electron is introduced into the central dot from source by successive tunneling events [the red arrows in Fig. 1(a)]. All other tunneling events are forbidden and, then, the system is stabilized in the (0, 1, 0) state. When the voltage is changed back to the low level, the charge state must return to (0, 0, 0), but the tunneling process is different. The electron in the central dot is removed to the drain by successive tunneling events [the blue arrows in Fig. 1(a)]. In this way, one electron is transferred from source to drain during one cycle of gate voltage, giving a current level of $e \times f$, where e is the elementary charge and f is the operation frequency.

We study analytically the overlap between (0, 0, 0) and (0, 1, 0) domains, the measure of turnstile operation, within the framework of the Coulomb blockade orthodox theory.[11] For quantitative measure of capability of turnstile operation, we define the normalized overlap, H_1/H_0, i.e., the V_{SD} extension of the overlap divided by the V_{SD} extension of the (0, 0, 0) domain, shown in Fig. 1(b). Figure 2 shows the stability diagrams analytically calculated for arrays of three dots having identical C_g's ($C_{g1}=C_{g2}=C_{g3}=1.2\times C_0$, with C_0 constant) for different dispersions in the $\{C_j\}$ arrangement of the four tunnel junctions in the array. In these examples, we set identical outer junction capacitances ($C_{j1}=C_{j4}$) and identical inner junction capacitances ($C_{j2}=C_{j3}$). Figure 2(a) shows the case of a uniform $\{C_j\}$ arrangement: $C_{j1}=C_{j2}=C_{j3}=C_{j4}=0.5\times C_0$. Figure 2(b) shows the case of a nonuniform $\{C_j\}$ arrangement: $C_{j1}=C_{j4}=0.425\times C_0$ and $C_{j2}=C_{j3}=0.575\times C_0$. It can be observed that, by making the outer junction capacitances smaller than the inner ones, as in Fig. 2(b), the overlap between (0, 0, 0) and (0, 1, 0) domains is increased. The larger overlap means the larger range of V_{SD} for turnstile operation and, therefore, it is more desirable.

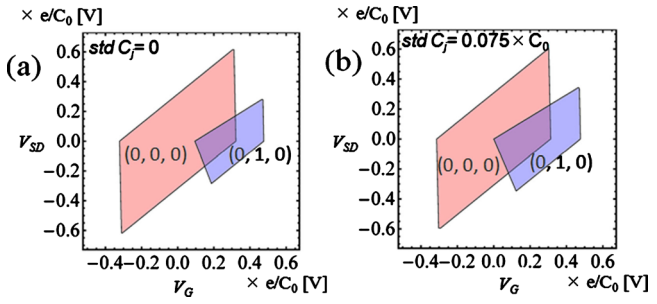

FIG. 2. (Color online) Stability diagrams in gate voltage (V_G)/source-drain bias (V_{SD}) plane showing the (0, 0, 0) and (0, 1, 0) stable charge domains calculated for arrays of three dots with identical C_g's, but different standard deviation of the $\{C_j\}$ distribution: (a) 0 and (b) $0.075\times C_0$ (S-L-L-S). Overlap of the two domains is increasing by increasing *std* C_j.

We evaluate the overlap as a function of both gate capacitances (C_g) and tunnel junction capacitances (C_j). In Figs. 3(a) and 3(b), we show the dependence of H_1/H_0 on the dispersion in $\{C_g\}$ and $\{C_j\}$, respectively. The normalized dispersion is defined as the coefficients of variation (cv) given by

$$cv\ \ C_g = \frac{std\ \ C_g}{C_g^{av}}; \quad cvC_j = \frac{std\ \ C_j}{C_j^{av}}, \tag{1}$$

where *std* C_g and *std* C_j are the standard deviations, and C_g^{av} and C_j^{av} are the average values of the $\{C_g\}$ and $\{C_j\}$, respectively. The coefficient of variation is used in this study because it allows us to compare the dispersion in $\{C_g\}$ and $\{C_j\}$ distributions relative to their average, C_g^{av} and C_j^{av}. In this analytical study, we also vary the ratios C_g^{av}/C_j in Fig. 3(a) and C_g/C_j^{av} in Fig. 3(b).

For Fig. 3(a), we plotted the effect of $\{C_g\}$ dispersion on the normalized overlap H_1/H_0, assuming uniform C_j's and $C_{g1}=C_{g3}$ (identical gate capacitances of the outer dots). The point, $cv\ C_g=0$, corresponds to identical (all-uniform) gate capacitances. When $C_{g2}<C_{g1}=C_{g3}$, the system is described as L-S-L, standing for large-small-large $\{C_g\}$ arrangement. When $C_{g2}>C_{g1}=C_{g3}$, the system is described as S-L-S, standing for small-large-small $\{C_g\}$ arrangement. It can be seen that, for any C_g^{av}/C_j, the overlap H_1/H_0 increases by increasing $cv\ C_g$ for S-L-S arrays. On the contrary, for L-S-L arrays, the overlap H_1/H_0 suddenly drops close to zero, indicating no overlap between (0, 0, 0) and (0, 1, 0) domains. This analytical finding supports our previous numerical results that S-L-S $\{C_g\}$ arrays always allow single-electron turnstile operation.[7] It should be also noted that this S-L-S structure is basically the same as the original turnstile design[2] in the limit of zero C_g's of the outer dots.

In Fig. 3(b), we plotted the effect of $\{C_j\}$ dispersion on the normalized overlap H_1/H_0, assuming identical C_g's for all dots, identical outer junction capacitances ($C_{j1}=C_{j4}$), and identical inner junction capacitances ($C_{j2}=C_{j3}$). The point, $cv\ C_j=0$, corresponds to identical (all-uniform) junction capacitances. When $C_{j2}=C_{j3}<C_{j1}=C_{j4}$, the system is described as L-S-S-L, standing for large-small-small-large $\{C_j\}$ arrangement. When $C_{j2}=C_{j3}>C_{j1}=C_{j4}$, the system is described as S-L-L-S, standing for small-large-large-small $\{C_j\}$ arrangement. It is observed that H_1/H_0 becomes larger for S-L-L-S structures, i.e., when the outer tunnel junction ca-

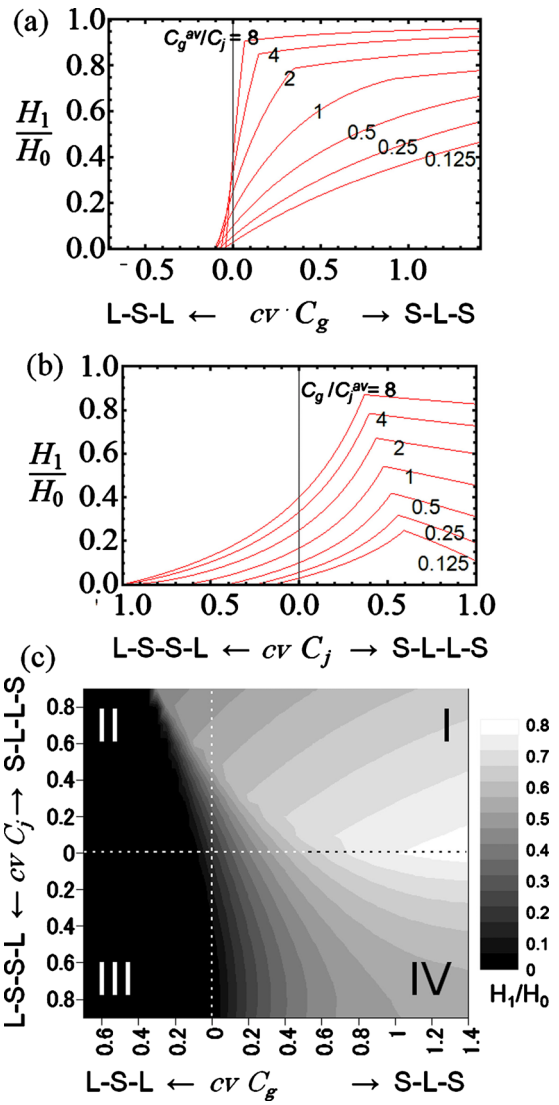

FIG. 3. (Color online) Dependence of the overlap (H_1/H_0) on the structural parameters of the quantum dot array. (a) For uniform C_j's and $C_{g1}=C_{g3}$ (gate capacitances of the outer dots), *cv* C_g is varied. When $C_{g2}<C_{g1}$, C_{g3}, the system is described as L-S-L (left side of the axis). When $C_{g2}>C_{g1}$, C_{g3}, the system is described as S-L-S (right side of the axis). C_g^{av}/C_j is used as parameter. (b) For uniform C_g's, $C_{j1}=C_{j4}$ (capacitances of the outer junctions), and $C_{j2}=C_{j3}$ (capacitances of the inner junctions), *cv* C_j is varied. When C_{j2}, $C_{j3}<C_{j1}$, C_{j4}, the system is described as L-S-S-L C_j arrangement (left side of the axis). When C_{j2}, $C_{j3}>C_{j1}$, C_{j4}, the system is described as S-L-L-S C_j arrangement (right side of the axis). C_g/C_j^{av} is used as parameter. (c) Contour plot of the overlap H_1/H_0 as a function of both *cv* C_g and *cv* C_j. Data is plotted for the case of $C_g^{av}/C_j^{av}=1$. Bright areas indicate high values of H_1/H_0, while dark areas correspond to $H_1/H_0=0$.

pacitances become smaller than the inner ones, although the transition of H_1/H_0 between L-S-S-L and S-L-L-S structures is smoother than in Fig. 3(a).

Figure 3(c) shows H_1/H_0 in the *cv* C_g-*cv* C_j plane for $C_g^{av}/C_j^{av}=1$. The contrast is defined in the range between 0 and 1: The bright areas correspond to high values of H_1/H_0, i.e., large overlap between (0, 0, 0) and (0, 1, 0) domains, while the darkest areas correspond to $H_1/H_0=0$, i.e., no overlap between (0, 0, 0) and (0, 1, 0) domains. The contour plot is divided into four regions, labeled I, II, III, and IV, depending on the $\{C_g\}$ and $\{C_j\}$ dispersion. The horizontal axis corresponds to *cv* C_g for the two opposite $\{C_g\}$ arrangements, i.e., S-L-S and L-S-L. Vertical axis corresponds to *cv* C_j for the two opposite $\{C_j\}$ arrangements, i.e., S-L-L-S and L-S-S-L. The axes intersection at *cv* $C_g=0$ and *cv* $C_j=0$ corresponds to uniform C_g's and uniform C_j's. Region I refers to structures with a larger C_g of the central dot and with outer junction capacitances smaller than the inner ones. In these conditions, H_1/H_0 is always nonzero, meaning that (0, 0, 0) and (0, 1, 0) domains always overlap. In region II, the overlap can be obtained only for a limited range of *cv* C_g and *cv* C_j. In region III, the overlap is practically zero. This means that arrays with C_g of the central dot smallest and outer junction capacitances larger than the inner ones are not suitable for single-electron turnstile operation. For structures in region IV, good conditions for single-electron turnstile can be again obtained, i.e., a finite overlap between (0, 0, 0) and (0, 1, 0) domains. These analytical results provide essential information about the evolution of the overlap as a function of the capacitance arrangements: The overlap between (0, 0, 0) and (0, 1, 0) domains is determined by both of $\{C_g\}$ and $\{C_j\}$ arrangements, although $\{C_g\}$ arrangement works more effectively. This is consistent with our previous numerical results[7] and provides a guideline for the design of single-electron turnstile devices. However, dot-gate capacitances C_g may be difficult to be externally controlled after device-fabrication, because C_g is determined by each dot size and relative position to the gate. On the other hand, as demonstrated in this section, we found that the arrangement of junction capacitances has also some effect on the turnstile conditions. We will show in Sec. III that, unlike dot-gate capacitances, junction capacitances are likely to be externally controlled, resulting in single-electron turnstile operation.

III. SINGLE-ELECTRON TURNSTILE IN DOPED SOI-FET

In this work, we propose a simple procedure for controlling the tunnel junction capacitances in a multidot array. The devices that we study are double-gate nanoscale SOI-FETs. The device structure is shown schematically in Fig. 4(a) (bird's eye view on left and top view on right). The device channel is defined by an electron beam lithography technique as a nanoscale constriction of typical width $w \approx 50$ nm and length $l \approx 100$ nm, connected to fan-shaped wider Si pads acting as source and drain. Top Si layer was uniformly doped with phosphorus from a spin-coated silica film containing P_2O_3. Doping concentration was estimated to be $N_d \approx 1 \times 10^{18}$ cm^{-3}. Thus, the channel region contains discretely distributed dopant atoms, which form a one-dimensional quantum dot array. We have recently demonstrated that each quantum dot may still be formed by individual dopants even in the presence of many other dopants in the channel.[12,13] The dots are coupled to each other by tunnel junctions formed in the Si segments between the active dopants.[9,10,14,15] The outer tunnel junctions, coupling the dot array to the electron reservoirs, are located in the pad areas in the immediate vicinity of the channel.

Two gates can control the potential in the channel: a front gate and a back gate. The Al front gate covers the channel area and a part of the fan-shaped adjacent pads

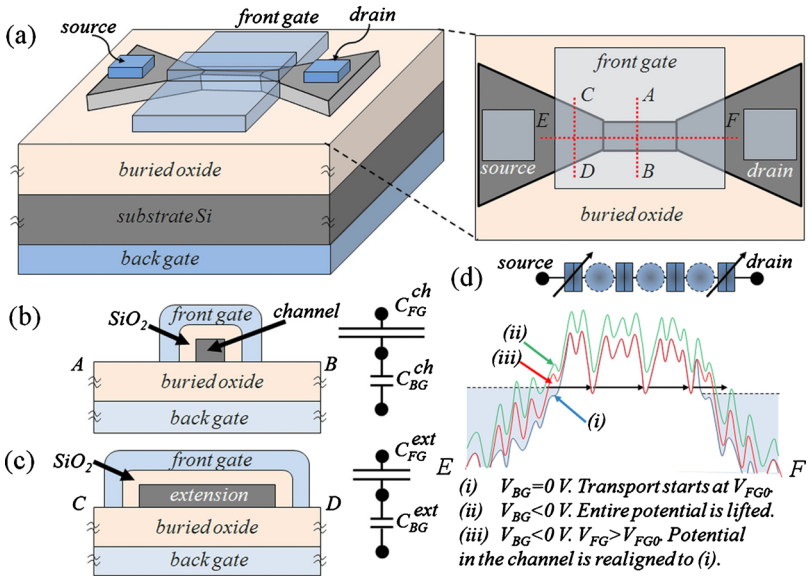

FIG. 4. (Color online) (a) Bird-eye view (left) and top view (right) of a SOI-FET. Channel is defined as the constriction connected to wider fan-shaped pads of Si. A front-gate and a back-gate control the potential in the thin (10 nm) top Si layer. [(b) and (c)] Cross-sectional views of device structure in the narrow channel region (along AB) and in the wider extension region (along CD), illustrating different electrostatic coupling to the front gate. (d) Potential profile from source to drain (along EF) showing an array of dopant-induced dots for three different front-gate voltage V_{FG}/back-gate voltage V_{BG} cases (indicated in the figure).

through a thermally-grown SiO_2 layer with thickness of $t_{ox}=10$ nm. The substrate Si (p-type) works as the back gate, coupled to the top Si through a buried oxide (*box*) layer with thickness of $t_{box}=400$ nm. The capacitive coupling of the channel to the front gate (C_{FG}) is much stronger than to the back gate (C_{BG}) because $t_{ox} \ll t_{box}$ and, furthermore, because the front gate surrounds the Si channel from 3 sides, as indicated in Fig. 4(b).

In the extension pad area near the channel [Fig. 4(c)], however, the coupling of the front gate is weaker than to the channel [Fig. 4(b)]. This is because the effect of the front-gate side walls is reduced as the width of the structure is increased. On the other hand, coupling of the back gate to the channel and to the pads is essentially the same. Therefore, using these asymmetric effects of the front gate and the back gate, it is likely that the outer junction capacitances can be effectively modulated.

A schematic example is shown in Fig. 4(d). We consider initially the situation in which the potential of the dot array is aligned with the source Fermi level at a certain front-gate voltage (V_{FG0}) for zero V_{BG}, as shown in case (i). If a negative back-gate voltage ($V_{BG}<0$ V) is applied, the potential is lifted up in the channel and in the pad areas near the channel, as illustrated in case (ii). The dot array potential can be realigned with source Fermi level by applying a more positive V_{FG}, as indicated in case (iii). The inner tunnel junction capacitances, coupling the dots to each other, are weakly sensitive to the back-gate/front-gate effect. However, for the end junctions at the fan-shaped areas, the front-gate coupling is much weaker than in the wire region because of the larger distance from the side walls. Therefore, the applied V_{FG}, which compensates the effect of V_{BG} on the junction capacitances in the wire region, cannot completely compensate this effect on the end junctions. When the barrier penetrates deeper inside the fan-shaped regions, both barrier width and barrier length become larger. Each of these two parameters affects the junction capacitance oppositely. However, the present experimental results indicate that the end junction capacitances are reduced independently of the inner junction capacitances. Although we may not exclude other possibilities, we suggest that the discrete dopant distribution affects also the potential in the fan-shaped region and the front of the junction is also dominated by one or only a few dopants. Therefore, the dominant effect of the front gate—back gate nonequivalent action is the increase in barrier width, which corresponds to a reduction in the end junction capacitances.

Figure 5(a) shows the source-drain current (I_{SD}) versus front-gate voltage (V_{FG}) characteristics measured at 17 K for two values of V_{BG} (0 and −5 V). We selected this doped-channel SOI-FET because, for $V_{BG}=0$ V, the characteristics exhibit a current peak with three subpeaks, which indicates the existence of a three-dot array in the channel.[16]

In Figs. 5(b) and 5(c), we show the effect of V_{BG} [0 V in (b) and −5 V in (c)] on measured charge stability diagrams (i.e., contour plots of I_{SD} in the space defined by source-drain bias, V_{SD} and front-gate voltage, V_{FG}). These results were previously reported in Ref. 10, but the mechanism was not clearly understood. The stability diagrams contain several diamond-shaped Coulomb blockade regions (light gray areas) with significant overlap. The current inside these regions is lower than the noise level in the measurements (<10 fA). We focus in Fig. 5 only on the first two observable domains, which can be associated with the charge state of "no excess electrons" and "one excess electron" in the dot array. The domains are roughly indicated in the figures by the guides for the eyes. These two domains correspond to the domains considered in our theoretical analysis, being essential for single-electron turnstile operation.

It can be seen that the overlap between the two domains becomes larger by applying more negative V_{BG}. In particular, the V_{SD} extension of the second stable charge domain increases for $V_{BG}=-5$ V. This behavior is the same as that of the analytically calculated stability diagrams, shown in Figs. 2(a) and 2(b): the second stable charge domain has a larger V_{SD} extension when outer junction capacitances are reduced compared to the inner ones. This confirms our expectation that negative V_{BG} leads to a decrease in the outer tunnel junction capacitances.

Figure 5(d) shows the source-drain current (I_{SD})/

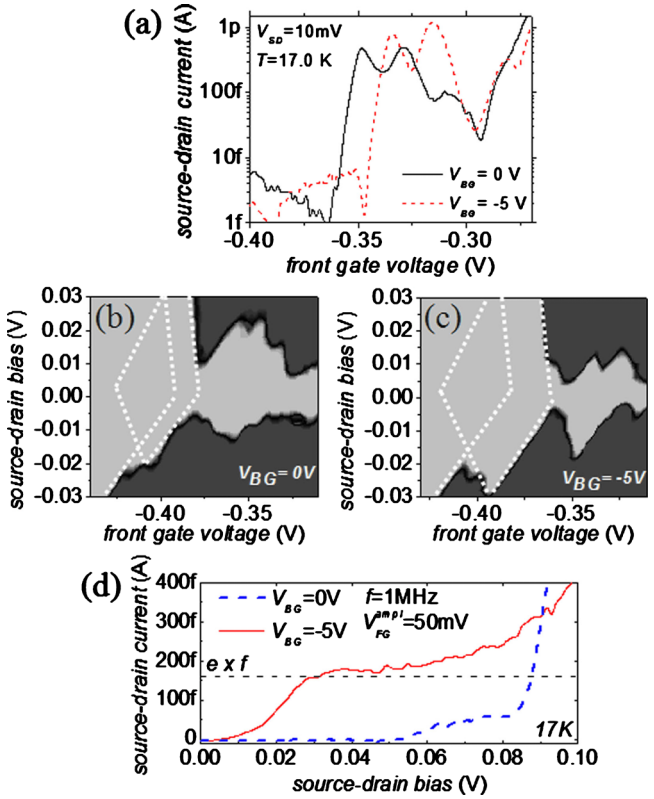

FIG. 5. (Color online) (a) Measured I_{SD}-V_{FG} characteristics for V_{BG}=0 V (solid line) and V_{BG}=−5 V (dashed line) at V_{SD}=10 mV. [(b) and (c)] Measured stability diagrams (contour plot of I_{SD} in the V_{SD}-V_{FG} space). Light gray areas corresponds to current I_{SD}<10 fA (noise level) and dark gray areas correspond to I_{SD}>50 fA. Back-gate voltage V_{BG} was changed as parameter: (b) 0 V and (c) −5 V. Guides for the eyes are drawn to roughly outline the first two stable charge domains. (d) I_{SD}-V_{SD} characteristics measured for V_{BG}=0 and −5 V while applying alternating V_{FG} (f =1 MHz, amplitude 50 mV). A current plateau at $e\times f$ can be observed for the case of V_{BG}=−5 V. All measurements were performed at a temperature T=17 K.

source-drain bias (V_{SD}) characteristics measured for V_{BG}=0 and −5 V by applying an alternating front-gate voltage V_{FG}. The V_{FG} pulse was set to a frequency f=1 MHz and a peak-to-peak amplitude of 50 mV, while the offset value was set inside the overlaps. With these conditions, we found that, for V_{BG}=−5 V, a current plateau well aligned at $e\times f$ level appears in the I_{SD}-V_{SD} characteristics, while such feature could not be found for V_{BG}=0 V. The $e\times f$ plateau means that electrons are transferred one-by-one from source to drain during every cycle of the V_{FG} pulse. Thus, single-electron turnstile operation was achieved by tuning the outer tunnel junction capacitances using the asymmetric front-gate/back-gate effect.

IV. SUMMARY

We have analytically investigated arrays of three quantum dots with a common gate. We introduced dispersion in dot-gate capacitances and tunnel junction capacitances and evaluated the overlap between two stable charge domains, i.e., (0, 0, 0) and (0, 1, 0), which is a necessary condition for single-electron turnstile operation. We found that the overlap can be enhanced by making the outer junction capacitances smaller than the inner junction capacitances. This is important because modification of junction capacitances is achievable after device-fabrication. In fact, we showed that, in SOI-FETs, the outer junction capacitances can be controlled using double-gate structure and we demonstrated single-electron turnstile operation. These results provide guidelines for realizing high-yield single-electron turnstile devices.

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