

Fabrication Method of Sub-100 nm Metal-Oxide-Semiconductor Field-Effect Transistor with Thick Gate Oxide

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Abstract

Based on the standard large-scale integrated circuit (LSI) process, sub-100 nm gate metal-oxide-semiconductor field-effect transistor (MOSFET) with thick gate oxide was fabricated. This was realized only by the modification of layout design, and no customization of the fabrication process was necessary. This unique designing technique is of great use in obtaining low-input-leakage MOSFET by advanced LSI process for high-performance analog applications.

As the size of metal-oxide-semiconductor field-effect transistor (MOSFET) is reduced, gate oxide thickness should also be reduced to suppress the short-channel effect¹⁾, and the leakage current through the gate oxide now becomes a concern not only in view of stand-by power consumption but also in view of input leakage for analog applications. For example, 90-nm gate MOSFETs typically have a gate oxide thickness of 1.5 to 1.9 nm, and the resultant gate oxide leakage reaches 10 pA to 10 nA/ μ m for the supply voltage of 1.2 to 1.5 V²⁾. Such large leakage currents cannot be acceptable in some analog applications like an electrometer or a charge amplifier³⁾, in which loss of input electrons must be minimized, and moreover shorter channel

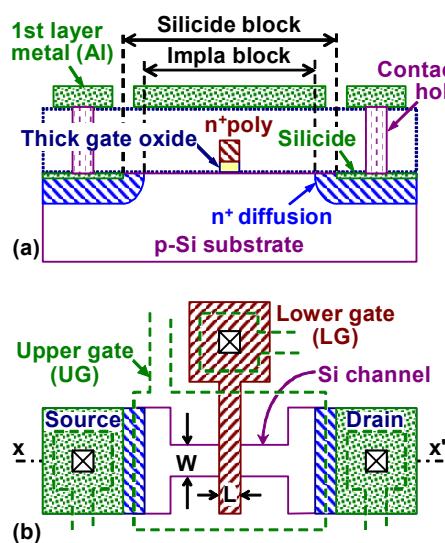


Fig. 1(a) Cross-sectional and (b) planar views of the proposed device. (a) corresponds to x-x' in (b).

length is desirable for higher charge sensitivity.

In order to realize short-channel MOSFETs with sufficiently thick gate oxide, the shallow inversion-layer source/drain is useful since the shallowness alleviates the requirement for the thin gate oxide¹⁾. However, previous proposals of such transistors⁴⁻⁶⁾ required special structure and fabrication procedure. Instead, within the framework of standard LSI process, we propose, as shown in Fig. 1, to utilize (1) thick gate oxide prepared for input/output circuits, (2) source/drain implantation and silicide blocks to clear the active area beside the lower gate from heavy doping, and (3) first-layer metal as an upper gate to induce shallow inversion layer. Since the metal wiring layer is used for upper gates, no additional process to the standard one is needed, but a certain degree of area penalty does exist, which may be circumvented by multilayer wiring.

Experimentally, n-channel test devices were fabricated with standard 65-nm LSI process. Specifically, 5-nm gate oxide for 2.5 V input/output circuits was selected to make the gate leakage negligible, lower gate length L was varied from 50 to 300 nm, channel width W was fixed at 300 nm, aluminum-based first-layer metal was used as the upper gate, and the premetal dielectrics below had an equivalent thickness of 440 nm (as per relative permittivity of 3.9). The devices were placed in a p-well, but the channel was not intentionally doped.

Figure 2 shows the subthreshold characteristics of the fabricated MOSFETs for various substrate (p-well) voltages V_{SUB} . Even for a short gate length of 60 nm, drain currents are cut off reasonably well thanks to the shallow inversion-layer source/drain. Note that the inversion-layer source/drain extends the use of 5-nm gate oxide by four process generations, as it was used with ordinary doped source/drain in 0.25-μm process. The behavior that the subthreshold swing becomes smaller for negative V_{SUB} is rather unique however, because the negative V_{SUB} usually results in the extension of source/drain depletion layer into the channel, reduced controllability of the gate on the channel potential, and larger subthreshold swing. For long-channel ($L= 250$ nm) device, subthreshold slopes shift almost parallel to the positive side as the negative V_{SUB} is applied, which is a natural consequence of the increased depletion layer charge below the channel. From this shift, effective

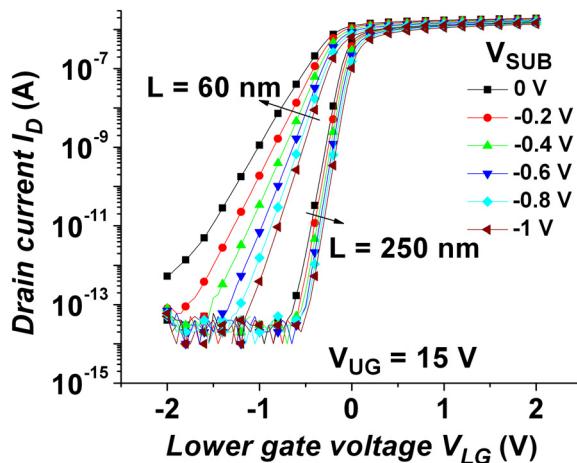


Fig. 2 Subthreshold characteristics of the fabricated devices for various substrate (p-well) voltages. Channel width is 300 nm, and drain and upper gate voltages are 50 mV and 15 V, respectively.

channel dopant concentration is calculated to be $9 \times 10^{16} \text{ cm}^{-3}$.

Figure 3 shows the threshold voltage roll off for different V_{SUB} 's. The threshold voltage roll off at short channel lengths is often explained by the charge sharing model^{7,8)}; the share of the gate in the depletion layer charge under the channel is reduced at short channel lengths due to the increased share of the source/drain depletion layer, resulting in the reduction (roll off) of the threshold voltage. The role off (and short-channel effect in general) is usually severe for negative V_{SUB} 's due to the lateral encroachment of the source/drain depletion layer. On the contrary, Fig. 3 shows smaller threshold voltage roll off for negative V_{SUB} . It was reported in ref. 5 that application of the subgate bias (equivalent to the upper gate bias in this report) lead to the shorter effective channel length L_{eff} . In association with this, application of negative V_{SUB} may result in a longer L_{eff} and relaxed short-channel effect. Actually, parallel shift of the roll-off curves for $\Delta V_{\text{Th}} < -380 \text{ mV}$ in Fig. 3 suggests that the channel length modulation is 15 nm or a little less for $V_{\text{SUB}} = -1 \text{ V}$.

Another important aspect of MOSFET characteristics is the series resistance, because the long extended inversion-layer source/drain has a large resistance. For the upper gate voltage of 15 V, the sheet channel resistance is around $15 \text{ k}\Omega$ leading to the series resistance of $7.5 \text{ k}\Omega\mu\text{m}$ per one side, i.e. source or drain side, with a $0.5\text{-}\mu\text{m}$ -long extended source/drain in this particular design. This cannot be acceptable in high-speed digital or high-power analog applications, but does not cause problem in many small-signal analog applications. For example, the MOSFET electrometer has an optimal biasing point at around threshold voltage based on the tradeoff between drain current sensitivity to input charge and noises in the drain current, as is shown in Fig. 8 of ref. 3.

In conclusion, the method of fabricating sub-100 nm gate MOSFET with 5-nm gate oxide by ordinary 65-nm LSI process was presented. It could be realized only by the modification of the layout design, and showed excellent short-channel characteristics down to the gate length of 50 nm. In addition, unique phenomenon of suppressed short-channel effect by the substrate bias was also observed. The proposed device is useful for high-performance analog applications, such as an electrometer and charge amplifier, which require low input-leakage current and high sensitivity at

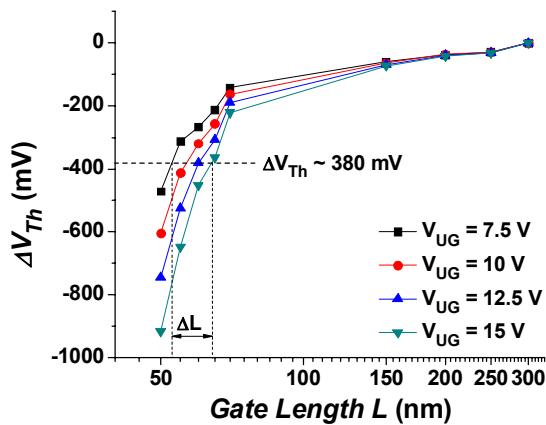


Fig. 3 Threshold voltage vs. gate length (roll off) under the same condition as in Fig. 2. Threshold voltages are defined at $0.1 \mu\text{A}$ of the drain current.

the same time.

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