Single-electron memory effect due to electron transfer between donors in Si field-effect transistors

DOCTOR THESIS

Single-electron memory effect due to electron transfer between donors in Si field-effect transistors

Si 電界効果トランジスタにおけるドナー間電子移動による単電子メモリ効果

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Abstract

Transistors have been significantly downsized over the past decades, reaching channel dimensions of around 100 nm. Thus, individual dopant atoms play a key role in the electrical characteristics of nanoscale field-effect transistors (FETs). In fact, it was revealed that a single isolated dopant works as a quantum dot (QD) at low temperatures and can mediate single-electron/single-hole tunneling. Even for nanoscale-channel FETs containing a large number of donors, single-electron tunneling is still mediated by one or only a few donors.

This unique behavior can be a frame model of a new type of electronic devices, such as a dopant-based memory device. Researches in this field have also been placing more emphasis on memory effects. Looking back in the history, research on single-electron device physics became very active in the 1990's. Since then, several memory operation modes have been proposed. However, to apply these devices in commercial electronics, some points must be addressed, such as low power consumption, small size (below 10 nm, which is required for room temperature Coulomb blockade operation).

As a first step towards dopant-based memory operation, in this study we focus on single-electron transfer between two donors in thin Si channel. When the donor is close to an insulator interface, which is the situation of thin-channel transistors, increasing gate voltage enhances the electric field in the channel and makes the

donor potential expand towards the interface. One electron can be thus confined inside the donor-interface QD, with the degree of hybridization dependent on the electric field and donor-interface distance. Under these conditions, the lateral confinement at the interface smoothly increases with increasing electric field. This suggests a gradual enhancement of the donor-gate capacitive coupling via the interface area. By considering this effect, we introduce a concept of voltage-dependent donor-gate capacitance in characterizing single-electron transport through donors in thin-channel transistors. We suggest that such capacitance variability can trigger electron exchange between neighboring donors, naturally located at different depths below interface. Single-electron tunneling current via one donor is used to monitor electron exchange with another nearby donor. Current jumps were observed as signatures of electron transfer.

We found that single electron transfer in a double-donor system is basically governed by the free energy of the system, but the kinetic effect of the tunnel resistances is responsible for the hysteresis. Thus, in a two-donor system, we demonstrated that memory effect can be obtained when considering variable donor-gate capacitances and kinetic effects.

In terms of stable memory operation, however, it is desirable to have a hysteresis controlled only by the system energy. For this purpose, we considered parallel asymmetric triple-donor systems. We found that hysteresis occurs by

trapping and detrapping in this system at different gate voltages due to the energy asymmetry in terms of electron transfer between the two end donors.

In summary, we demonstrated single-electron transfer in double- and triple-donor systems. In case of double-donor systems, we found that hysteresis is generated by a kinetic delay of electron transfer. It should be noted that, for variable donor-gate capacitance, only one electron can be involved in the transfer process. In contrast, for fixed donor-gate capacitance, double-electron occupancy triggers an electron to transfer to the next donor. For triple-donor systems, we found that hysteresis is controlled only by the free energy of the system, which can be promising for developing applications to memory devices.

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Chapter 1
Introduction
1.1 Research background
1.1.1 CMOS Technology

The rapid growth of the semiconductor industry in the past 40 years has largely been a result of the ever-decreasing size of CMOS (complementary metal-oxide semiconductor) switching elements, which form the underlying logic circuits in practically every modern digital system. As the size of CMOS switches and of the field-effect transistors from which they are made is reduced, integrated circuits constructed from these devices improve in speed, device density, and cost per function. The result is an intense industrial drive toward miniaturization, as predicted by Moore [1]. The International Roadmap for semiconductors predicts that CMOS transistors with gate lengths of 7 nm will be mass-produced by 2018 [2]. Devices with channel lengths of 45 nm are already in production, and individual research devices with channel lengths of 4 nm have been demonstrated [3]. CMOS devices will continue to shrink over the next two decades, but as they approach the scale of the silicon lattice, the precise atomic configuration of their structure will become critically important to their macroscopic properties. Mead and Keyes recognized in the 1970s [4], [5] that below a critical size, devices can no longer be described, designed, modeled, or understood as continuous

semiconductors with smooth boundaries and interfaces.

At nanometer scale dimensions, the number and position of the dopant atoms, introduced to alter the electrical properties of regions of a field effect transistor, will vary between devices and, as a result, each transistor will be microscopically different. The variation in dopant positions between devices leads to measurable differences in macroscopic parameters, such as drive current, threshold voltage, and leakage. Further size reduction reduces the number of dopants, exacerbating the variations and hence the differences in device performance. Furthermore, with decreasing device size, the interface roughness of typical gate oxides (one or two atomic layers) becomes comparable to the gate thickness itself. Thus, each device will have a unique gate thickness and a unique pattern of interface roughness. The use of high-permittivity (high-k) gate insulators as a replacement for present gate oxides will allow thicker gates, which may ease this source of variation for one or two technology generations (3 to 6 years). However, atomic-scale variation in the positions of impurity atoms, local variations in the silicon/silicon dioxide interface above the channel, and local variations of the thickness of the silicon dioxide introduce, between each transistor and its neighbor, fluctuations in device electrostatics, electron transport, and gate leakage, respectively. The granularity of the photo-resist used to pattern the gate will introduce further local variations in the shape of the gate itself. With existing technology, it is impractical to image the

detailed atomic structure of individual nanometer-scale CMOS transistors and to link their structure to the corresponding device characteristics.

Over the past decade, researchers aiming for an understanding of intrinsic parameter fluctuations in nanometer-scale CMOS transistors have therefore resorted to numerical simulation, using increasingly detailed mathematical models. Wong and Taur were the first to report a full 3D simulation of field-effect transistors under the influence of random discrete doping [6]. They used a drift-diffusion simulator, which models electron transport as incompressible fluid flow, considering the area under the gate as a checkerboard of smaller, interconnected devices, each with a different density of dopant atoms. The results showed the two classic fingerprints of randomly distributed, discrete dopants: a spread in the device threshold voltages, and a lowering of the mean threshold voltage relative to that of a continuously doped system (the formation of percolation paths will always allow current to flow at a lower gate potential than for an idealized device). Yet in the past few years, the same device scaling that proves so problematic to simulate has led to radical improvements in computational power. Combined with modern, highly parallel simulation codes, this means that statistical simulations that ran for weeks in the late 1990s can now be completed in a weekend. Present simulation tools are still mainly drift diffusion–based and now include random distributions of dopants in the channel, source, drain, and gate of a field effect transistor. In

addition, variations in gate thickness and atomic-scale roughness in the pattern of the gate edges are accounted for, and the quantum nature of channel electrons is modeled through a density gradient adjustment to the device's potential profiles. There is even a move to replace the drift-diffusion core of modern commercial and research device simulation codes with the computationally more expensive Monte Carlo approach to correctly account for electron transport at the high lateral fields present in modern devices in the on-state [7]. However, threshold voltage variations and the sub-threshold operation of devices (which govern device leakage) remain the most important parameters for a circuit designer, and these can be adequately modeled with drift diffusion simulators. Now that rapid, robust, and accurate simulation tools have been developed, a wealth of applications presents themselves in the fields of electronic devices, circuits, and systems. For instance, such simulations may help to develop devices that are resistant to fluctuation effects. Double-gate transistors (in which a 10-nm silicon channel is gated above and below) require no channel doping and are therefore immune to dopant fluctuation effects, but are subject to body thickness variations due to local roughness above and below the channel. The new simulation tools are being used to predict when industry should move to double-gate transistors, and when double-gate transistors themselves will become unviable. In addition, methodologies have been developed to make use of the extracted data on fluctuations as an input to industrial circuit

design tools [8]. For the first time, circuit designers can quantitatively analyze how atomic-scale variations in field-effect transistors will affect the yield and functionality of commercial digital logic and memory circuits.

1.1.2 Single-electron tunneling device

Single-electron tunneling devices (SETs) may be produced in a number of different ways, the most common being metallic islands or semiconducting quantum dots. The basic operation (Figure 1.1) requires an island of electrons with a capacitance C which is small enough so that the charging energy for the island (e^2/C) is much larger than the thermal fluctuations in the system (k_BT). Electrons may only flow through the circuit by tunneling onto the first unoccupied energy level, μ_{N+1}. Therefore, electrons will only flow one by one if the bias voltage, V, is increased such that $\mu_l > \mu_{N+1} > \mu_r$ or a gate is used to change the electrostatic potential of the island to produce the same tunneling conditions.

Numerous memory circuits based on SETs have been suggested and some of them have been demonstrated at helium liquid temperature and at 40 K [9]; these are aimed at low power consumption, rather than high-speed applications. The first uses binary decision diagrams to produce an AND gate, while the second uses oscillatory characteristics of a multiple gate SET transistor to produce a XOR gate.

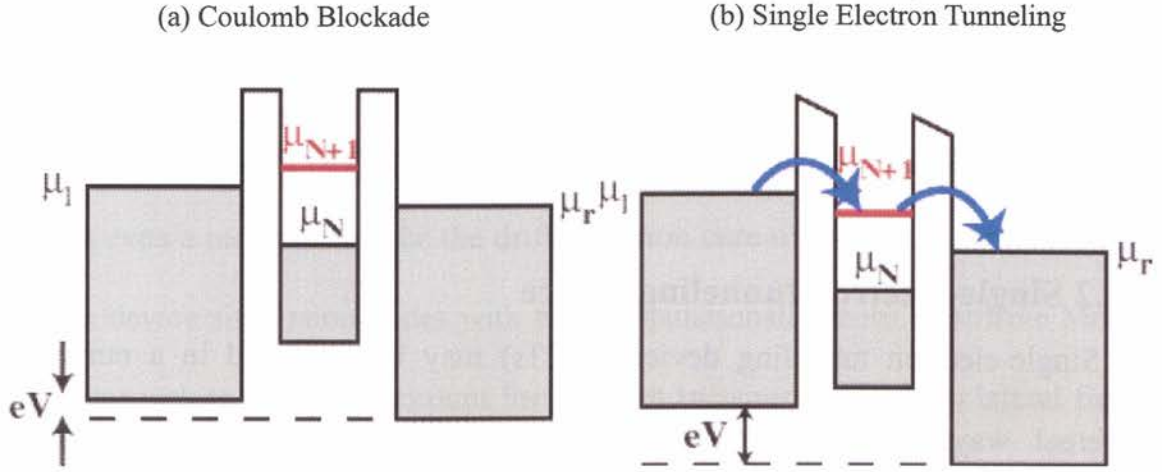


Fig.1. 1 For an island of total capacitance C with N electrons, with μ_N the chemical potential of the highest filled electron state, μ_{N+1} the chemical potential of the first available empty state for an electron, and μ_l and μ_r the chemical potentials of the left and right electrodes, respectively, it may be shown that the energy to add an electron to the island is $\mu_{N+1}-\mu = e^2/C$. Therefore, provided $e^2/C \gg k_BT$ (i.e., C is small) and the tunneling resistance, $R_T \gg R_K = 25.8k$ (i.e., the electron wave function may be localized on the island), for a voltage V applied across the electrodes, no electrons may flow if $\mu_{N+1} > \mu_l$ and μ_r - the state known as Coulomb blockade (a). If a larger bias is applied across the electrodes, such that $\mu_l > \mu_{N+1} > \mu_r$, then empty states may be populated in the island and single electrons may tunnel through the island (b). A gate may be used to change the Fermi level of the island and therefore switch the single electron current on or off.

SET devices are at present believed to be useful predominantly for memory, electrometer and metrology applications. To make a SET device operational at room temperature, it is estimated that the charging energy of the island (e^2/C) should exceed the thermal energy k_BT by at least a factor of 10. This suggests that the island of the SET device must be of the order of 10 nm. For reliable circuit operation, however, e^2/C should exceed the thermal energy k_BT by a much larger factor and hence the feature sizes must be smaller than 10 nm. Simulations of complete SET circuits using a conventional type of architecture and incorporating

perturbation by background charge fluctuations suggest that it will be necessary to go to dimensions of the order of 2 nm, and that liquid nitrogen cooling may be necessary. The feature dimension will therefore depend on the control of the background charge fluctuations. Recent calculations suggest that quantum dot array structures (such as multiple tunnel junctions) are less susceptible to disorder and background charge effects [10]. The energy needed to read or write a bit and the frequency of the circuits are limited by the uncertainty principle, $\Delta E \cdot \Delta t \geq h$. To prevent bit errors, the circuit cannot operate too close to the minimum uncertainty product.

There are three important limits, which determine the ultimate performance of such systems, in particular the thermal limit, the quantum limit, and the power dissipation limit (Figure 1.2). The energy necessary to write a bit determines the thermal limit. This energy must be bigger than the average energy of the thermal fluctuations, $k_B T$, otherwise bit errors will occur.

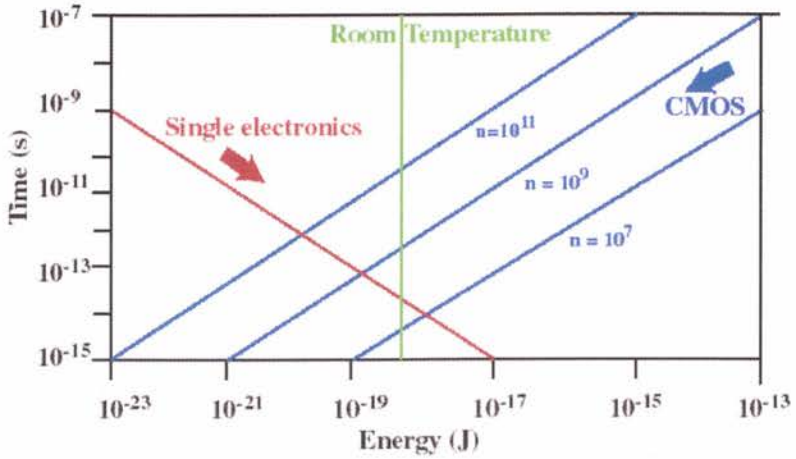


Fig.1. 2 An energy - delay diagram for single electronics. Room temperature operation can only be achieved to the right of the line labeled "room temperature". The lower left-hand corner of the diagram is inaccessible due to quantum fluctuations and the lower right-hand corner of the diagram is inaccessible due to dissipation. The dissipation limit is represented by three lines, each corresponding to a different device density, n. The current trends in CMOS and single electronics are indicated in the diagram [11].

For the present SET circuits, this energy is 10^{-22} J (10^{-3} eV), which corresponds to a temperature of 10 K. The trend in SET circuits is to increase this energy and thereby to increase the operating temperature of the circuits. The optimum value for the energy to write a bit for room temperature operation is about 4 x 10^{-19} J (2 eV), which is a factor of 100 greater than k_BT. In principle, the speed of SETs is limited by the RC time constant that, for capacitances of 1 aF, corresponds to a switching speed of 0.1 ps. To take advantage of these speeds, however, the logic architecture would have to be local, so that the SETs would not have to drive a high capacitance line across the chip. Logic circuits that would possibly be based on local architectures, such as binary decision diagram (BDD) logic or cellular automata,

are theoretically and experimentally under investigation. In practice, when a SET device has to drive an external load, such as a word or bit line in a memory cell, there are RC delays that limit the operating frequency and it is likely that even using graded tunnel barriers in a poly-silicon type device, only sub-ns access times may be achieved. Due to the high impedance required for Coulomb blockade, SET devices are easier to implement into memory structures, than logic circuits [12].

1.2 Overview of our previous work towards single dopant electronics

1.2.1 Observation of dopant potential in Silicon by LT-KFM

In nanoscale FETs, it is crucial to monitor the discrete dopant distribution. We developed for that purpose a technique of a low-temperature Kelvin probe force microscope (LT-KFM) that allows us to monitor the electronic potential profiles at the surface of doped-nanoscale-channel FETs [13], [14]. In the conventional KFM technique [15], a conducting cantilever is scanned over the sample surface at constant height. At each measurement point, the electrostatic force that builds up between the cantilever and the sample is nullified by a dc voltage that corresponds to the actual time-averaged surface electronic potential. KFM can thus sense electrostatic force through thermally-grown SiO_2 layer due to charges not only at the channel surface, but also a few nanometers below the interface. Such depth

sensitivity of KFM is a strong advantage over other dopant mapping techniques, since one can monitor changes in potential profiles almost simultaneously while the device is working. In fact, in our previous works [13], [14], we have already shown that, in conventionally-doped silicon FETs ($N_d = 1\times10^{18}$ cm^{-3}), individual ionized dopants can be identified.

We show that LT-KFM is a powerful tool for observing individual dopants, and also it allows detection of single-electron filling in dopant potentials. We fabricated SOI-FETs with P-doped top Si layer covered by a thin (~2 nm) thermally-grown SiO_2 film. Top Si was patterned into a small constriction channel coupled to wider pads of Si for source and drain. Side gates and a back gate can be used to control the channel potential. Device structure and setup are shown in Figure 1.3 (a). In order to observe the dopant-induced potential landscape, it is necessary to deplete the channel of free carriers that could screen the dopant potentials. For that, we perform the measurements at low temperature (13.7 K), and, therefore, most dopants (donors) are neutralized without thermal emission of electrons under low electric fields. However, the substrate Si and two side gates were commonly biased at V_G = -4 V, which is large enough to deplete the donor electrons and to observe the bare donor ions without screening by the carrier electrons. The KFM scanning area is 120×120 nm^2 centered on the constriction channel, practically covering 80% of the channel width. Figure 1.3 (b) shows the electronic potential map measured at

source-drain bias V_{SD} = 0 mV. The contrast is defined so that higher electronic potential (larger negatively charged) areas correspond to brighter contrast. The non-uniform potential is due to the presence of ionized P impurities [16]. We counted a number of 90~120 fine potential fluctuations (dark spots) with radii of 2~4 nm and depths of 10~30 mV in the measured KFM images. This value is in good agreement with the estimated number of dopants located within about 5 nm from the surface in the scanning area.

The spatial extension of the dark spots is comparable to the Bohr radius for P in Si of 2.3~3 nm [17], [18], [19], suggesting that they may originate from single dopant atoms. The potential depth is less than 46 meV which is the first binding energy of a P dopant in bulk Si [20]. However, since KFM monitors the potential at the surface of the channel, the observed values of 10~30 mV may correspond to ionized dopants located few nanometers below the surface. For the results shown in Figure 1.3 (b), channel is depleted of free carriers by a negatively-large gate voltage (V_G = -4 V) and also source-drain bias is zero (V_{SD} = 0 mV). In this system, we then apply small source-drain biases (V_{SD} = 1 mV (Figure 1.3 (c)) and V_{SD} = 5 mV (Figure 1.3 (d)), corresponding to continuous flow of electrons at source-drain currents I_{SD} = 1 nA and I_{SD} = 10 nA, respectively.

The potential maps change as a result of electron trapping and electron flowing through dopants. From these measurements, we cannot clearly identify the actual

conduction path. However, in order to distinguish single-electron trapping events, we focus on the encircled region that contains the lowest potential observed in the channel at $V_{SD} = 0$ mV. It is most likely that electrons will occupy this low-potential region. Line profiles taken in this area are shown in Figure 1.3 (e). In order to remove the effect of background potential changes, we added 5 mV and 10 mV to the line profiles for $V_{SD} = 1$ mV and $V_{SD} = 5$ mV, respectively. The displacement is possibly due the long range effect of charging in the vicinity of the region of interest. This way, the line profiles were aligned and we observed that the potential minimum is increased by 22 mV for $V_{SD} = 1$ mV and by 21 mV for $V_{SD} = 5$ mV. Considering the localization of these potential increments and their values, we ascribe each of these observations to single-electron trapping events (event #1 and event #2 in Figure 1.3 (e)) in two different neighboring dopants located at about 5 nm distance from each other. These results suggest that even in many-dopant systems, single-electron/single-dopant interactions can be distinguished [21]. Further understanding of single-electron charging in highly-doped nanoscale FETs can be achieved by studying the electronic potential maps under the application of varying electric fields.

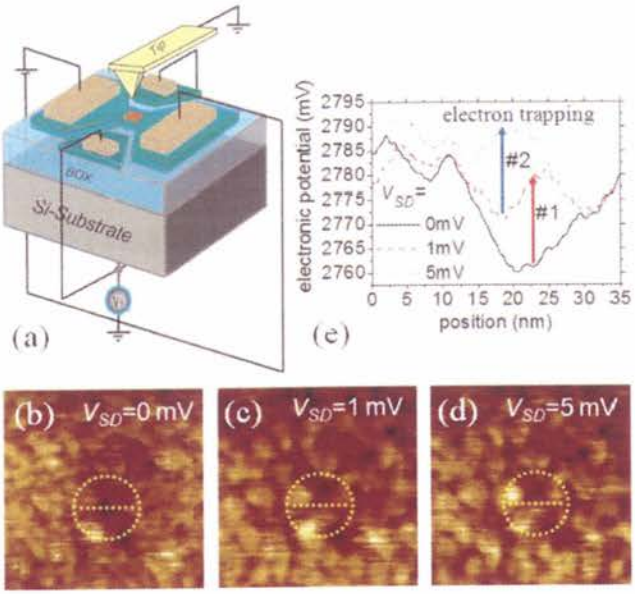


Fig.1. 3 (a) Schematic LT-KFM measurement setup and SOI-FET structure. **(b)-(d)** Surface potential maps (120×120 nm^2) for V_G = -4 V and different values of V_{SD} (0, 1, and 5 mV). Dark spots can be ascribed to ionized phosphorus dopants. **(e)** Line profiles (as marked on the maps) indicate localized potential jumps under current flow, evidence of single-electron filling in dopants.

1.2.2 Single-electron turnstile using dopants

A single-electron turnstile is a device able to shift exactly one electron between two electrodes during each cycle of an ac gate voltage. In the original design, single-electron turnstile consists of a chain of three metallic QDs with a single ac gate coupled to the central one [22]. The device operation is based on single-electron tunneling according to the Coulomb blockade orthodox theory [23]. From a practical viewpoint, silicon devices are preferable for single-electron transfer. It has been demonstrated that single-dot single-electron transistors (SETs) can operate

as single-electron transfer devices [24]. However, for that purpose, two phase-correlated ac gates were used to control the conductance of the two tunnel barriers connecting the dot to the leads. More recently, we have demonstrated that single-electron turnstile can be achieved in doped silicon nanowire SETs made in silicon-on-insulator (SOI) substrates using only one ac gate [25], [26].

Under ac operation, in some devices individual electrons were transferred one at a time between leads through the irregular potential landscape created by discrete dopants. In these devices, QDs are formed by individual dopants or clusters of dopants, not by lithography. For single-electron turnstile operation, it is necessary to use devices that work as a 3-QD array [22]. We found such devices based on the sub-structure of the first peak (Figure 1.4 (a-b)) and we measured the charge stability diagrams (Coulomb diamonds) close to the onset of the conduction. In Figure 1.4 (c)-(d), the left-most Coulomb domains are shown with guides for the eyes that indicate the estimated boundaries of these domains. These domains are most important for single-electron turnstile operation because of their large extension in V_{SD}. For these two regions it can be also noticed that the domain extension and the overlap is modified by V_{BG}. The second observable domain becomes larger and creates a better overlap with the first domain for V_{BG} = -5 V compared with V_{BG} = 0 V. At the same time, wide ranges of V_{FG} are available inside the stable domains on the left and right sides of the overlap, which allows us to set

the low and high levels of the ac V_{FG} pulse with sufficient certainty.

In order to evaluate the turnstile operation, we measured I_{SD}-V_{SD} characteristics by applying an ac V_{FG} (f =1 MHz, peak-to-peak amplitude of 50 mV) across the overlap region. Plateau at $I_{sd} = e \times f$ (with e the elementary charge and f the operation frequency) should be observed as an indication of a single-electron per V_{FG} cycle being shifted from source to drain. As shown in Figure 1.4 (e), only the curve measured for V_{BG}=-5 V shows the expected plateau with a current level very close to $e \times f$, extending for about 40 mV in V_{SD}. Current in the plateau region is proportional to operation frequency ($I_{SD} \approx e \times f$), confirming the single-electron turnstile operation. These results prove the capability of conventionally-doped nanowire SOI-FETs to be utilized as tunable single-electron turnstile devices working with discrete dopants.

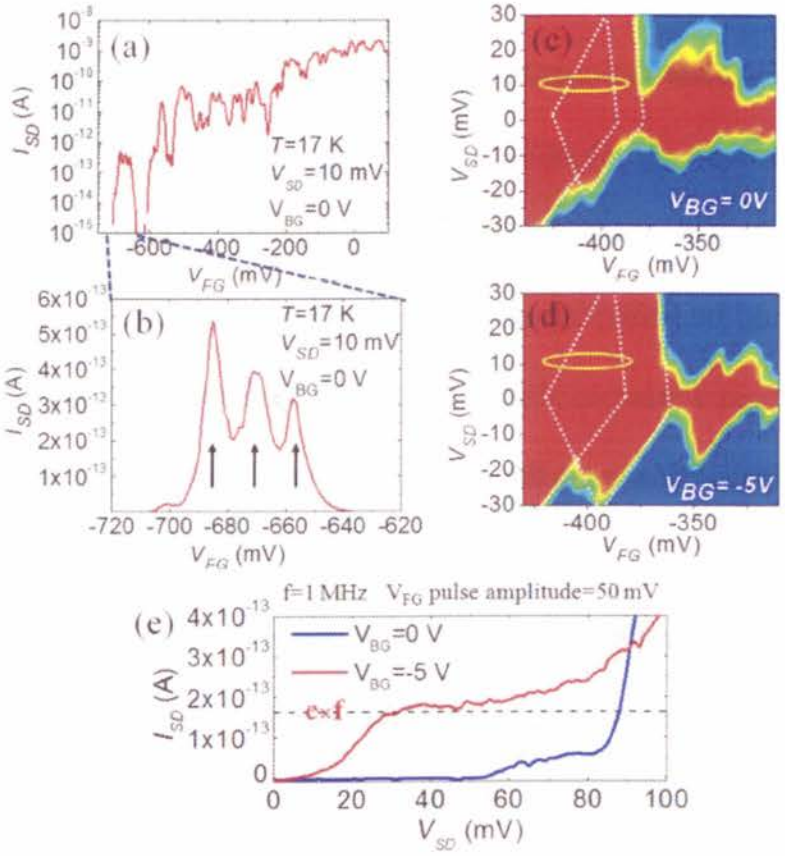


Fig.1. 4 (a)-(b) I_{SD}-V_{FG} characteristics measured for small V_{SD} and low temperatures (full characteristics and first current peak as inset). **(c), (d)** Charge stability diagrams (contour plots of I_{SD} in the space defined by V_{FG} and V_{SD}) for two values of V_{BG}: 0 and, respectively, -5 V. Current is practically zero in the marked areas. An ac V_{FG} was applied across the overlap of the two domains. **(e)** I_{SD}-V_{SD} characteristics measured under ac V_{FG}. An $e \times f$ plateau can be observed for V_{BG} = -5 V.

1.2.3 Single-photon detection using dopants

Single photon detection has attracted an increasing interest in the frame of new applications, such as quantum cryptography [27]. So far, photomultiplier tubes and Si avalanche photo-diodes are the most widely employed devices to detect single-photon. More recently, quantum dots (QDs) have become attractive alternatives

since they do not require avalanche multiplication processes to detect single photon. QD single-photon detection has been first reported for GaAs/AlGaAs field-effect-transistor (FET) containing a layer of InAs QDs. We have also demonstrated single-photon detection using two-dimensional (2D) Si multi-dots FET [28], with the dots created by nanoscale local oxidation of Si (nano-LOCOS) [29]. In our devices, detection of single photon relies on the capture of single photo-excited carrier by a QD, leading to measurable fluctuations of the current in a percolation path with tunnel-coupled QDs.

We recently showed that the principle of single-photon detection can be extended to arrays of QDs naturally formed by ionized dopants in the channel of nanoscale FETs, [30]. We investigated for that purpose SOI-FETs with the same structure as the devices described in the previous sections, but without Al front gate to allow direct illumination of the device channel. Back gate voltage (V_{BG}) is used to control the channel potential. We studied as a first step the effect of visible monochromatic light (450~750 nm) on the SET electrical characteristics. We observed that continuous light illumination induces noisy pattern superposed on the single-electron tunneling current peaks in the I_{SD}-V_{BG} characteristics (Figure 1.5, top). When measured as a function of time (Figure 1.5, bottom), I_{SD} RTS with mainly two levels appears, suggesting the detection of a single photon after photo-excitation of an electron-hole pair and electron trapping in a dopant potential well.

The number of RTS is proportional to the number of photons absorbed in the channel, suggesting that the RTS is photon-induced. The above results are encouraging for developing new devices based on the interaction between quanta of charge, light and atomic entities in nanoscale.

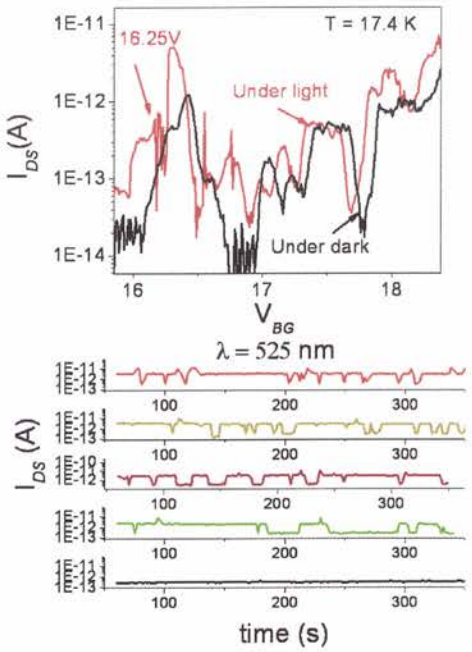


Fig.1. 5 Top: First peak of I_{SD}-V_{BG} characteristics measured in dark and under continuous light illumination (λ=525 nm). Noisy features under light are indicated. Bottom: I_{SD}-*time* measurement for V_{BG}=16.25 V, for increasing incident photon flux (from bottom to top). RTS with mainly two levels appears, with frequency increasing with incident photon flux.

1.3 Purpose of this work

As we discussed above, continuous miniaturization of silicon field-effect transistors is accompanied by a strong reduction of the number of dopants

incorporated in the device channel. Random distribution of dopants in the device channel has significant effects on the device characteristics. From a different viewpoint, the technological advance associated with this trend opens the possibility for a single dopant atom to become the active unit of future electronic devices.

In this thesis, we propose a novel concept of memory effect, in which single-electron memory nodes are dopant-induced QDs formed in the doped-channel of nanoscale FETs. Single-electron tunneling current through one or a few dopants can be utilized as a very sensitive detector of charging events in the nano-channel. This concept can provide the grounds for developing a compact atomic memory for future electronics.

To evaluate dopant-based memory effect, we proceeded through the following steps:

1. We have studied single-electron transfer in phosphorous doped-channel SOI FETs, with characteristics similar to those described in the previous section. We measured the I_{SD}-V_G characteristics at low temperatures (~15 K) by sweeping V_G around the first observable current peak, upwards (increasing V_G) and, successively, downwards (decreasing V_G).

2. Drain current verses time (I_{SD}-*time*) measurements have been carried out and

features that can be considered as signatures of single-electron trap by a single dopant have been observed.

3. Finally, we used Monte-Carlo Coulomb blockade simulation to prove our experimental results. We introduced a voltage-dependent donor-gate capacitance concept by which only a single electron can be trapped by a single dopant, resulting in single-dopant memory device operation.

1.4 Thesis outline

These studies are described in this thesis, which contains seven chapters.

Chapter 1 gives an introduction to fundamental research on dopant-based electronic devices, together with an overview of our recent work towards memory physics.

In Chapter 2, a review of the literature related to single-electron memory devices is presented. Furthermore, a conceptual model of single-dopant memory device will be explained. The device consists basically of two donors, where one donor works as conduction path, while the other works as single-electron trap. The aims of the research are outlined.

In Chapter 3, silicon nanodevice fabrication process and device structure are first discussed. Simulated potential profiles and electrical characteristics are explained. From the I-V characteristics we observed a fine hysteresis between upward and downward sweeps, which is a signature of a single-electron trapping by a single donor in the thin (10 nm) Si channel.

In Chapter 4, I introduce a theoretical treatment for investigating the electrical properties of double-donor systems based on Coulomb blockade orthodox theory. I reproduce a fine hysteresis which is good agreement with experiments. I introduce a new concept of gate-voltage dependent donor-gate capacitances. I show that

single-electron transfer between two donors is only possible if the gate capacitances of the two donors cross over, by considering the behavior of donors near interfaces.

In Chapter 5, I investigate triple-donor systems. We also reproduce a fine hysteresis by 3-dot system, which can be ascribed to energetically-controlled transfer of one electron between donors.

Chapter 6 contains conclusions to research and provides suggestions for appropriate directions for future research in the area.

Chapter 2
Memory Devices

This chapter presents the basic concepts and physics of operation of all the nonvolatile semiconductor memory types. We will first present the basic principles and history of nonvolatile memory (NVM) devices in Section 2.1. A review of the single-electron memory devices in use today is given in Section 2.2 and is concluded by a rather general comparison of the different types of memory concepts. Finally, Section 2.3 discusses a novel concept of single-dopant memory device.

2.1 Conventional memory devices

The basic operating principle of nonvolatile semiconductor memory devices is storage of charges in the gate insulator of a MOSFET, as illustrated in Figure 2.1.

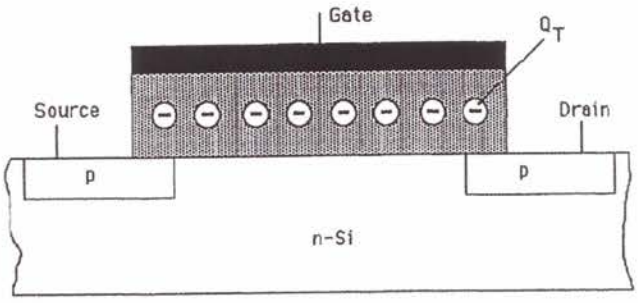


Fig. 2. 1 Basic operating principle of nonvolatile semiconductor memory: the storage of charges in the gate insulator of a MOSFET.

If one can store charges in the insulator of a MOSFET, the threshold voltage of the

transistor can be modified to switch between two distinct values, conventionally denned as the 0 or erased state and the 1 or written (programmed) state, as illustrated in Figure 2.2. From the basic theory of the MOS transistor, the threshold voltage is given by

$$V_{TH} = 2\varphi + \varphi_{ms} - \frac{Q_I}{C_I} - \frac{Q_D}{C_I} - \frac{Q_T}{\epsilon_I} d_I \ldots\ldots\ldots\ldots\ldots\ldots 1.1$$

φ_{MS} = the work function difference between the gate and bulk material.

φ_F = the fermipotential of the semiconductor at the surface.

Q_I = the fixed charge at the silicon or insulator interface.

Q_D = the charge in the silicon depletion layer.

Q_T = the charge stored in the gate insulator at a distance d_I from the gate.

ϵ_I = the dielectric constant of the insulator.

C_I = the capacitance of the insulator layer.

Thus, the threshold voltage shift, caused by the storage of the charge Q_T is given by

$$\Delta V_{TH} = -\frac{Q_T}{\epsilon_I} d_I \ldots\ldots\ldots\ldots\ldots\ldots 1.2$$

The information content of the device is detected by applying a gate voltage V_{read} with a value between the two possible threshold voltages. In one state, the transistor is conducting current, while, in the other, the transistor is cut off. When the power supply is interrupted, the charge should, of course, remain stored in the gate

insulator in order to provide a nonvolatile device. The storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes.

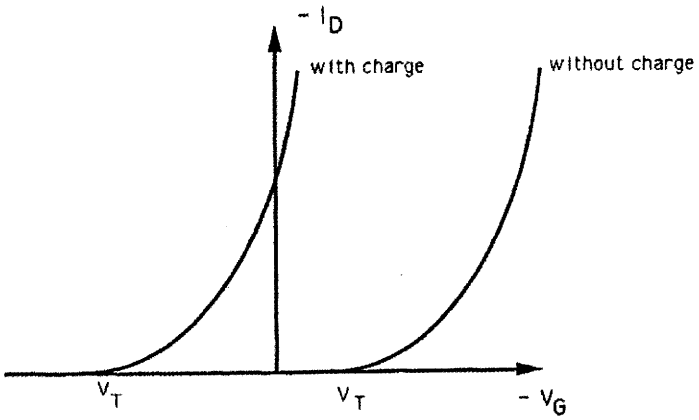


Fig. 2. 2 Influence of charge in the gate dielectric on the threshold of a p-channel transistor.

The first class of devices is based on the storage of charge on a conducting or semiconducting layer that is completely surrounded by a dielectric, usually thermal oxide, as shown on Figure 2.3 (a). Since this layer acts as a completely electrically isolated gate, this type of device is commonly referred to as a floating gate device [32]. In the second class of devices, the charge is stored in discrete trapping centers of an appropriate dielectric layer. These devices are, therefore, usually referred to as charge-trapping devices. The most successful device in this category is the MNOS device (metal-nitride-oxide-semiconductor) structure [32], in which the insulator consists of a silicon nitride layer on top of a very thin silicon oxide layer,

as shown in figure 2.3 (b). Other possibilities, such as Al_2O_3 (MAOS) and Ta_2O_5 (MTOS) [33], [34], have never been successfully exploited.

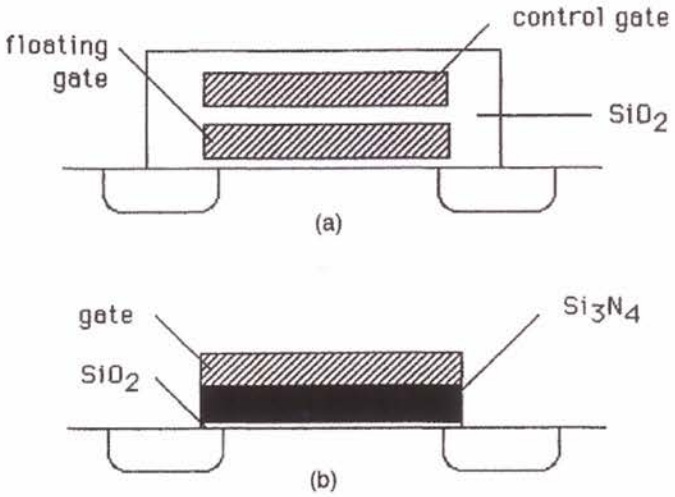


Fig. 2. 3 Two classes of nonvolatile semiconductor memory devices: (a) floating gate devices; (b) charge-trapping devices (MNOS device).

2.2 Single-electron memory devices

2.2.1 Recent developments

Nano-flash devices are basically three terminal devices where a floating gate is charged and the charge produces a large change in the threshold voltage of the transistor channel. The design allows an intermediate operation between DRAM and Coulomb blockade, potentially allowing higher density than DRAM at lower power and higher operating temperatures. In addition, nonvolatile DRAM-like memories based on the Coulomb blockade effect are intensively investigated. Both Hitachi's PLED [35], and Likharev's NOVORAM are prominent examples [36], [37]. The key issue is the creation of extremely flexible tunnel barriers, for instance

by multiple barriers or sandwiched barriers.

In 1994, K. Yano reported 2 terminal devices where information is stored in deep traps in poly-Si. The devices are created on a 3 nm thick Si film using 0.25 μm technology, where one or more dots are formed naturally in the vicinity of a FET in which trapped charge modulates the threshold voltage of the FET [38]. The device can be operated at room temperature and has been integrated in very large-scale memories (128 Mb in 8k x 8k x 2 units of which half was operational), although it is not certain if Coulomb blockade is of any relevance for device operation.

One of the major problems of this type of memory is relying on the natural formation of dots and the resulting poor control of device characteristics. This may be a major hurdle to manufacturability. The advantage is a small cell size of $2F^2$, one quarter of a folded-data line DRAM cell size. Since 1994, at least three major companies have introduced technologies for room temperature Coulomb blockade memory cells [39], [40], [41], [42]. They are compatible with CMOS process and integration on 250 nm technology level was demonstrated in one case [38]. Their properties place these memories between today's DRAM and flash EEPROM. Hitachi presented the first single-electron-based integrated circuit by making an 8 × 8 memory cell with read/write operation. The operation voltage is 15 V and the device is based on ultra-thin poly silicon wires (3 nm x 100 nm), in which the

memory node consists of an isolated poly-grain representing a potential well. The presence of charge in this well modulates the conductance of naturally formed current paths between the grains. Because of the compatibility with "classical" silicon processing these results offer a real breakthrough. The device operating principle, however, relies upon the statistics within the poly-wire. Recently, Hitachi extended this technology to demonstrate a 128 Mb SET memory using 0.25 μm CMOS processing.

2.2.2 Major challenges and difficulties

- Background charge fluctuations remain the biggest technological bottleneck. In order to reduce the perturbation of these effects on SET circuits, the critical dimension must be on the order of 2 nm. Unless significant progress can be made in controlling the background charges, it seems unlikely that Coulomb blockade circuits can be integrated on a large scale.

- The required uniformity of devices is extremely demanding, raising doubts if they can be manufactured with the required tolerances at a reasonable price.

- Even assuming that large scale integration is possible, solutions must be found on how to overcome the electrostatic interactions between devices.

- Error tolerance for Coulomb blockade devices has not been investigated in great detail, but it seems likely that, in order to have adequate tolerances, the device must operate either at lower temperature or higher voltage (and hence power).

Due to these difficulties, SET appears to be, for the present, far from being an alternative to CMOS. Only time will demonstrate if the technological bottlenecks can be overcome and perhaps nano-flash devices may bridge the gap between MOSFETs and SET.

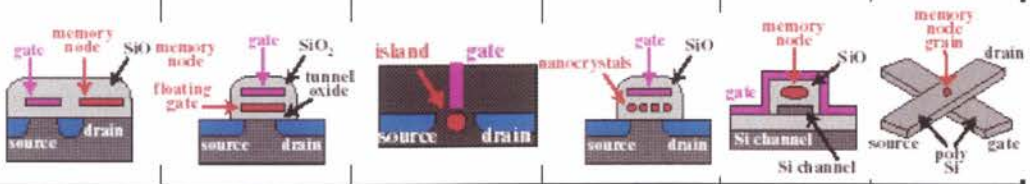
	Conventional Memory		Quantum Dot Memory			
	DRAM	Flash	SET	Nano-flash		Yano-type
				Multidot	Single dot	
device structure						
read time	~10 ns	~10 ns	1 ns	~10 ns	~10ns	~20 μs
write time	~10 ns	~1 ms	1 ns	~100 ns	<1 μs	~10 μs
erase time	< 1nm	~1ms	< 1nm	~1 ms	<1 ms	~10 μs
retention time	~1 s	~10 years	~ 1s	~1 week	~5 s	~1 day
endurance cycles	infinite	10^4	infinite	10^6	10^6	10^7
operating voltage	3 V	15 V	1 V	5 V	10 V	15 V
voltage for state inversion	0.2 V	~5 V	< 0.1 V	0.65 V	0.1 V	0.5 V
electron number to write bit	10^5	10^3	1 (excluding no to change gate potential)	10^3	1 (excluding no to change gate potential)	2 (excluding no to change gate potential)
cell size	~12 F^2/bit	~9F^2/bit	9-12 F^2/bit	9F^2/bit	9F^2/bit	2F^2/bit

Fig. 2. 4 Performance comparison among conventional and QDs memories (modified after data from Hitachi Cambridge Laboratory).

Figure 2.4 is an extract of the tables in Annex I and compares conventional DRAM and flash memory with known data from a number of SET based quantum dot memory devices from the literature. The schematics demonstrate that most of the SET devices are really small-scale examples of conventional DRAM or flash memory, so that the capacitance of the memory node is small enough to produce single-electron effects. Most of the proposed and realized SET memories store

information in gain cells rather than the conventional DRAM 1T cells, which on one hand is an intrinsic advantage, but on the other complicates direct comparison between these memory technologies.

2.3 Single -dopant memory devices

2.3.1 Introduction

As a consequence of the fast-paced downscaling of silicon field-effect transistors (FETs), the number of dopants in the channel is strongly reduced. Even one dopant can significantly affect device characteristics. Electrical measurements of nanoscale transistors containing one isolated dopant have recently revealed the properties of single-charge transport mediated by a donor [43], [44] or an acceptor [45]. Placing exactly one dopant in nanoscale with sufficient accuracy remains, however, an important challenge for device fabrication and controllability.

We recently demonstrated that individual dopants can be electrically accessed even when the nanoscale channel contains a large number of dopants [20]. In such dopant-rich environment, the long-range Coulomb potentials of all donors cumulate, significantly lowering the potential of one or only a few dopants relative to the others. These few dopants can work as conduction path for single electrons when a gate voltage aligns their potential with the source Fermi level. By using a low-temperature Kelvin probe force microscope, we were able to observe the potentials of individual ionized dopants [13], [14], [20] as well as the localized single-

electron charging in neighboring donors [20]. Electrical measurements of a statistical number of doped-channel nanoscale FETs have also shown the effects of channel geometry on the donor-induced potential profiles [20], giving a guideline for fabricating single-dopant devices in dopant-rich nanostructures.

In this work, we propose a new concept of a *dopant-based single-electron memory*. A memory unit consists of a memory node, in which charge can be trapped, and a sensor to read out the charge state of the memory node. We suggest that single-electron current mediated by individual dopants in nanoscale-channel FETs can be used as a sensor for observing trapping in neighboring dopant-induced traps [46]. This concept is first briefly described conceptually, then results of electrical measurements that indicate charging at the level of individual traps will be shown.

2.4 A conceptual model

An ionized donor in Si can be treated in a first approximation as a hydrogenic potential well [16]. For bulk Si, the ground state of a phosphorus donor is located 44 meV below the conduction band edge, while the Bohr radius is estimated to be around 3 nm. Such a donor can work as a nanoscale quantum dot (QD), with dimensions much smaller than present capabilities of lithographic techniques. One electron added into this QD induces a significant charging energy, precluding the addition of a second electron. This is basically the Coulomb blockade effect that

has been the basis for the development of single-electron transistors [47].

In fact, a donor can practically accommodate only one electron. When two donors are found close to each other, as illustrated in Figure 2.5, two Coulomb potential wells are formed and an electron can be transferred between the donor wells. Assuming that one of the donors is well coupled to electrodes (source and drain), it will work as the single-electron current path. The other donor can, on the other hand, significantly influence the current by trapping one electron, due to the electrostatic coupling of the two donor-QDs. Thus, one can use the single-electron current to monitor the charge state of the satellite donor.

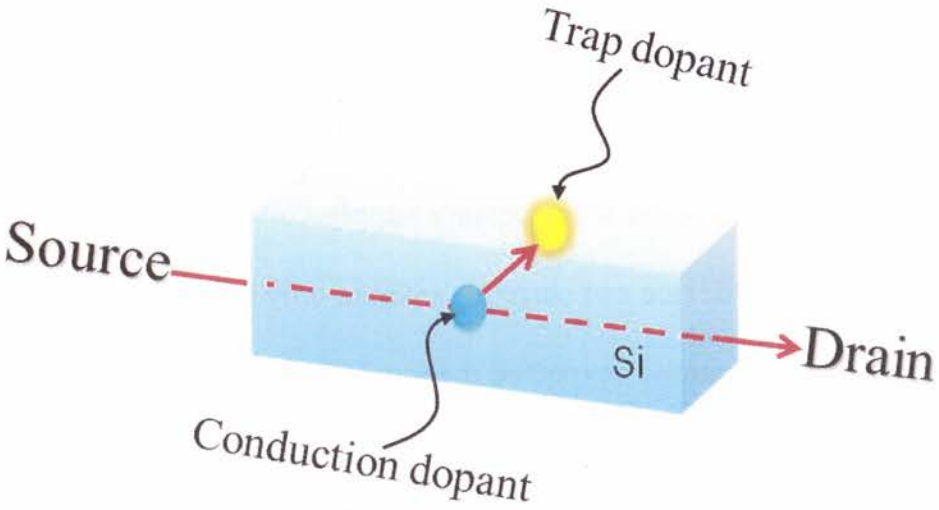


Fig. 2. 5 A schematic view of a two-donor single-electron memory system. One donor works as conduction path (indicated by the horizontal arrows), while the other works as single-electron trap.

2.5 Advantages of single-dopant memory devices

There is an emerging demand for simultaneous high performance and very low power dissipation to achieve miniaturized personal electronics, like personal digital assistants (PDA's), which are the next driving force of the electronics industry. For example, to achieve a PDA capable of recognizing speech and convert it into text, 100 000 MIPS/W is required. Here MIPS/W is proportional to the product of the number of electrons needed to operate a logic gate and the supply voltage. Dramatically reducing the supply voltage is difficult because it is limited by temperature and threshold voltage variations. Therefore, the only way to achieve a quantum leap in MIPS/W is to dramatically reduce the number of electrons representing one bit.

Our proposed single-dopant memory device may able to represent one bit just by one electron and as a result the necessary supply voltage may be low. However, single-dopant memory device can currently operate only at low temperature (15 K). Room temperature operation is expected theoretically in a nm-size device [48], [49], and conduction through an STM tip above a nanometer scale practical has been shown to be affected by single-electron charging, even at room temperature [50]. However, it is still believed that the time at which such a device can function properly at room temperature is a long way off.

Conclusion

If we look into what happened in the last ten years, memory-cell technology has continuously changed, including the emergence of flash memory technology and ferroelectric-film memory technology. This can be interpreted as the memory technology still having plenty of room with which to play, and innovations are strongly desired from the user side of storage needs. This aspect is further emphasized if we look at the fact that our way of storing information is rapidly changing from the older regime, relying on papers and other analog electronic means, to the digital regime in the multimedia era. This might create new needs of storing information, significantly different from the older specifications in bandwidth, storage capacity, power consumption, and so on.

Chapter 3
Device structure and experimental setup

3.1 Introduction

Single-electron tunneling and the Coulomb blockade effect have been observed in a variety of materials. Silicon devices are, however, preferable due to the well-developed Si technology. Furthermore, utilizing naturally-formed Coulomb potential wells introduced by individual atoms (dopants) allows us to overcome present limitations of nanolithography. This extreme case may allow the incorporation of physics of single-electron/single-atom interaction into useful electronic devices. In the following, we will describe basic physics of electron transfer phenomenon between donors for realizing applications such as single-dopant memory device.

3.2 Device structure

The devices are similar to those explained in details in the previous sections and were fabricated on silicon-on-insulator (SOI) substrates, as schematically shown in Figure 3.1. They have a channel defined by an electron beam lithography technique as a constriction of around 70 nm in length and 50 nm in width, connected to wider pads of Si for source and drain, as shown in the SEM image in Figure 3.2. The top Si was uniformly doped with phosphorus diffused from a spin-coated silica film containing phosphorus oxide (P_2O_3). The top Si is separated by a

400-nm-thick buried oxide. Doping concentration was estimated to be $N_d \approx 1\sim3\times10^{18}$ cm^{-3}, which corresponds to an inter-dopant distance of 7~10 nm. We estimated this value from SIMS (Secondary Ion Mass Spectrometry) depth profiles of control samples fabricated by the same doping treatments as the device samples, as shown in Figure 3.3. A 10-nm-thick SiO_2 layer was then thermally grown, making the final thickness of the Si channel around 10 nm. Aluminum pads were then deposited and patterned to form the gate, source, and drain pads.

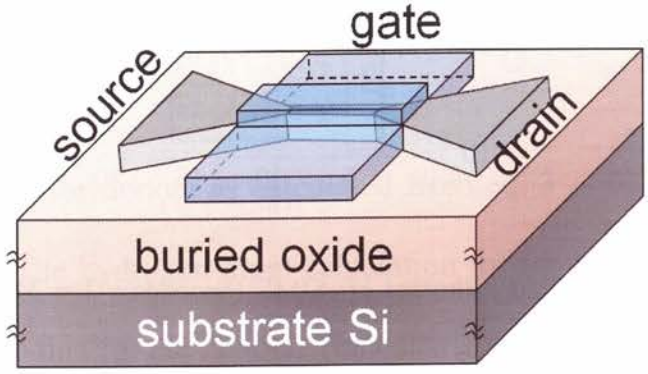


Fig.3. 1 Schematic device structure of SOI-FET.

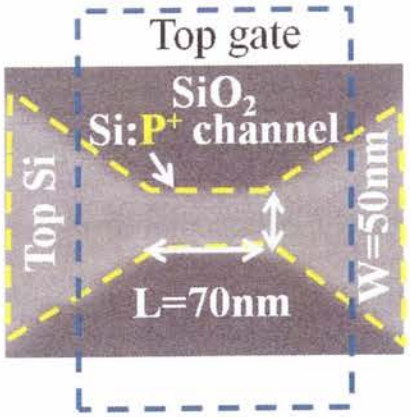


Fig.3. 2 SEM (Scanning electron microscope) image of the MOSFET device channel.

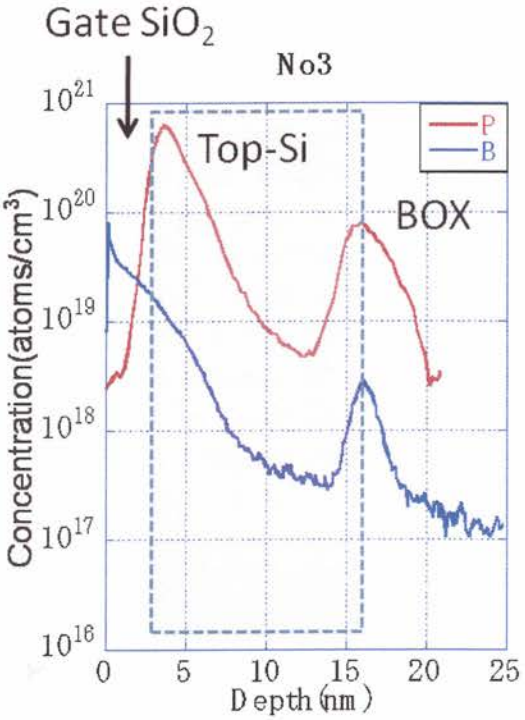


Fig.3. 3 Doping concentration estimated by SIMS (Secondary Ion Mass Spectrometer) for a reference sample.

3.3 Dopants in Silicon

When a semiconductor is doped with donor or acceptor impurities, impurity energy levels are introduced that usually lie within the energy gap. A donor impurity has a donor level which is defined as being neutral if filled by an electron, and positive if empty. Conversely, an acceptor level is neutral if empty and negative if filled by an electron. These energy levels are important in calculating the fraction of dopants being ionized, or electrically active. To get a feeling of the magnitude of the impurity ionization energy, we use the simplest calculation based on the

hydrogen-atom model. The ionization energy for the hydrogen atom in vacuum is:

$$E_H = \frac{m_0 q^4}{32\pi^2 \varepsilon_0^2 \hbar^2} = 13.6\text{eV} \ldots\ldots\ldots\ldots\ldots\ldots 1$$

The ionization energy for a donor (E_C - E_D) in a lattice can be obtained by replacing m_o by the conductivity effective mass of electrons.

$$m_{ce} = 3\left(\frac{1}{m_1^*} + \frac{1}{m_2^*} + \frac{1}{m_3^*}\right)^{-1} \ldots\ldots\ldots 2$$

and by replacing ε_0, by the permittivity of the semiconductor ε_s in eq.1 :

$$E_C - E_D = \left(\frac{\varepsilon_0}{\varepsilon_S}\right)^2 \left(\frac{m_{ce}}{m_0}\right) E_H \ldots\ldots\ldots\ldots\ldots\ldots 3$$

The ionization energy for donors as calculated from eq. 3 is 0.025 eV for Si and 0.007 eV for GaAs. The hydrogen-atom calculation for the ionization level for the acceptors is similar to that for the donors. The calculated acceptor ionization energy (measured from the valence-band edge, E_a = (E_A- E_V) is 0.05 eV for Si and GaAs. Although this simple hydrogen-atom model given above certainly cannot account for the details of ionization energy, particularly the deep levels in semiconductor [51], [52], [53], the calculated values do predict the correct order of magnitude of the true ionization energies for shallow impurities. These calculated values are shown to be much smaller than the energy gap, and often are referred to as shallow impurities if they are close to the band edges. Also, since these small ionization energies are comparable to the thermal energy k_BT, ionization is usually complete at

room temperature. Figure 3.4 shows the measured ionization energies for various impurities in Si.

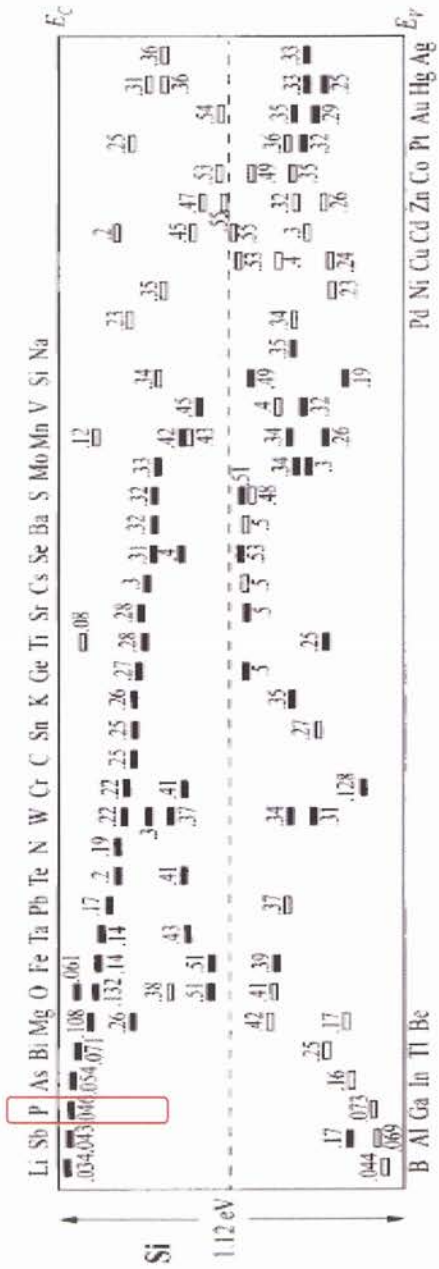


Fig.3. 4 Measured ionization energies for varies impurities in Si
(Physics of Semiconductor devices、S. M. Sze, p23, 3rd edition)

3.4 Numerical simulation of dopant-induced potential distribution in Si channel

Effects of randomness on device characteristics have recently been studied both experimentally and theoretically [54], [55], [56], [57]. Fluctuations of characteristics are caused not only by variation in the average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. Moreover, fluctuations are particularly pronounced as the spatial scale of doping and oxide thickness variations become comparable with the dimensions of devices [55], [58]. The International Technology Roadmap for Semiconductors has forecasted a transition from conventional bulk devices to silicon-on-insulator (SOI) devices, and then to multiple-gate SOIs as high-performance devices [59]. Diverse computational approaches, such as small signal analysis [60], [61], [62], drift-diffusion (DD) [63], [64], and Monte Carlo simulation [65], [66], [67], have recently been reported to study fluctuation-related issues in semiconductor devices.

I use a simple simulation method to observe the fluctuations due to dopant potentials in Si channel. In this simulation, it was assumed that every dopant introduces a Coulomb-shape potential into the mesh according to the equation [16]:

$$P = \frac{-e \times \tanh(\lambda r)}{4\pi\varepsilon r} \ldots (16)$$

Where p is a potential, e is an elementary charge, r is a distance from the charge. Regarding the Coulomb-like potential around an individual ionized dopant, the singularity was smoothed away by using the potential with a characteristic length scale $1/\lambda$ = 2.75 nm, giving a well depth of 44 meV. These parameters are comparable to the Bohr radius a_0 = 1.9 nm and to shallow dopant ionization energies. The diameter and shape of potential fluctuations induced by individual dopants are shown in Figure 3.5.

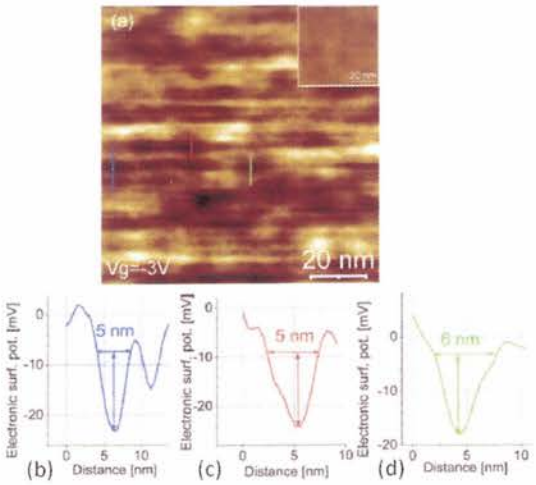


Fig.3. 5 Surface potential map of the channel area obtained by KFM at 13K. (a-c) The profiles of local potential fluctiaon induced by individual phosphorous atoms measurend by KFM [13].

Figure 3.6 (a) show the case when one phosphorous donor is placed close to the surface in a Si device channel. Next, by applying gate voltage electron will be emitted from the dopant as a result of dopant ionization. Figure 3.6 (b) shows the simulated potential profile for an ionized dopant in Si. The Coulomb-shaped potential around the dopant is clearly visible. The minimum value of the potential is

equal to -44 meV which reflects the ionization energy of phosphorous in Si.

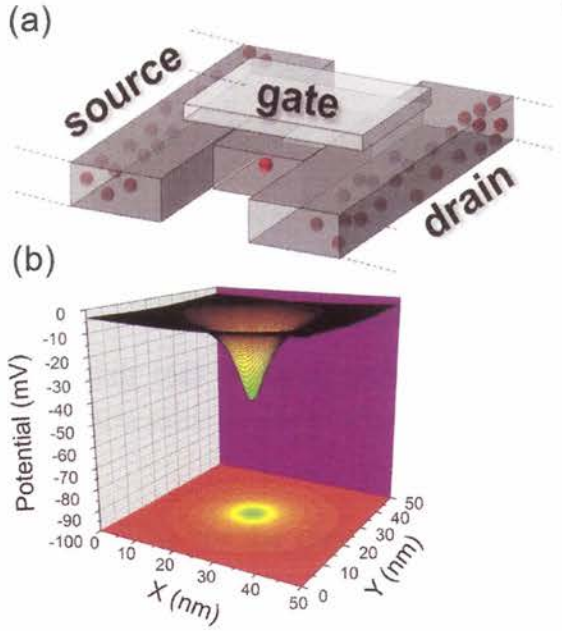


Fig.3. 6 (a) One ionized phosphorous donors located in Si channel. **(b)** Potential profile for one ionized phosphorous donors in Si

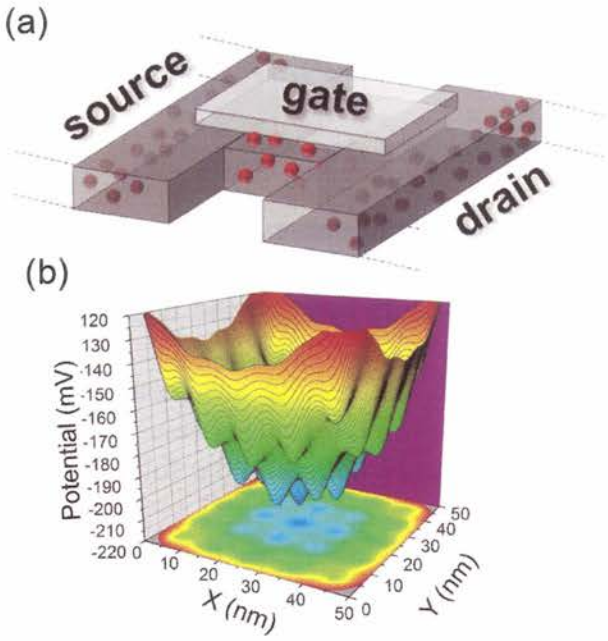


Fig.3. 7 (a) Many ionized phosphorous donor located in Si channel. (b) Potential profile for many ionized phosphorous donor in Si.

However, the above idealistic case of one isolated dopant is far from reality. It is reasonable to assume that in real devices some dopants are close enough to interact with each other. Dopants which are far from each other can be treated as two different potential dips. However, as the distance between two dopants is decreased, Coulomb potentials of both ions start to overlap and, as a consequence, the potential barrier between the dopants also decreases. This fact has very important meaning for the carrier transport in Silicon nanowire.

As we increase the number of dopants in the Si channel, as schematically

shown in figure 3.7 (a), the overall potential landscape is modulated by the superposed potentials of many dopants [13], [16], [68]. For nanostructures doped with phosphorus (P), the lowest electronic potential will be formed close to the channel center due to the entire set of dopants. When the channel minimum conduction band energy is shifted close to the source Fermi level by gate voltage, transport occurs through the dopant-induced QDs and a first peak appears. In my experiment, the results are most prominent on the first peak, a fact that I will explain in more details in the following chapter.

3.5 Electrical characterization of Si:P nanowire

3.5.1 Measurement setup

For investigation of single-electron transfer through phosphorous-doped SOI-FETs, we observed the gate-voltage versus source-drain current (I_{SD} -V_G) characteristics for a large number of devices. The schematic device structure and measurement setup are shown in Figure 3.8.

The I_{SD}-V_G characteristics were measured using an HP precision semiconductor parameter analyzer. The devices were mounted in the chamber of the parameter analyzer and all the measurements were performed under vacuum conditions.

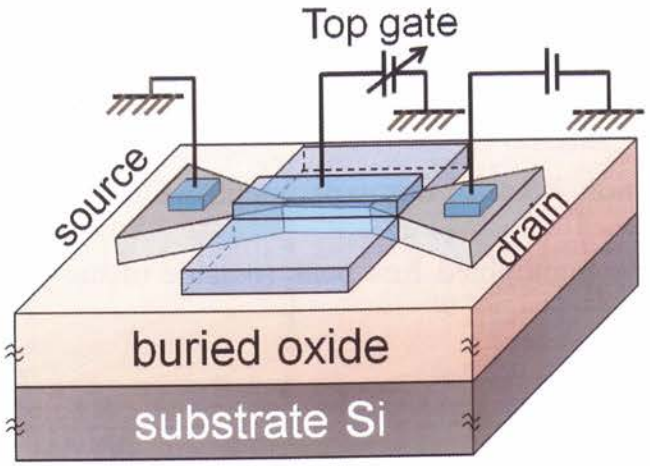


Fig.3. 8 Schematic device structure and biasing circuit for measuring the I_{SD}- V_G characteristics.

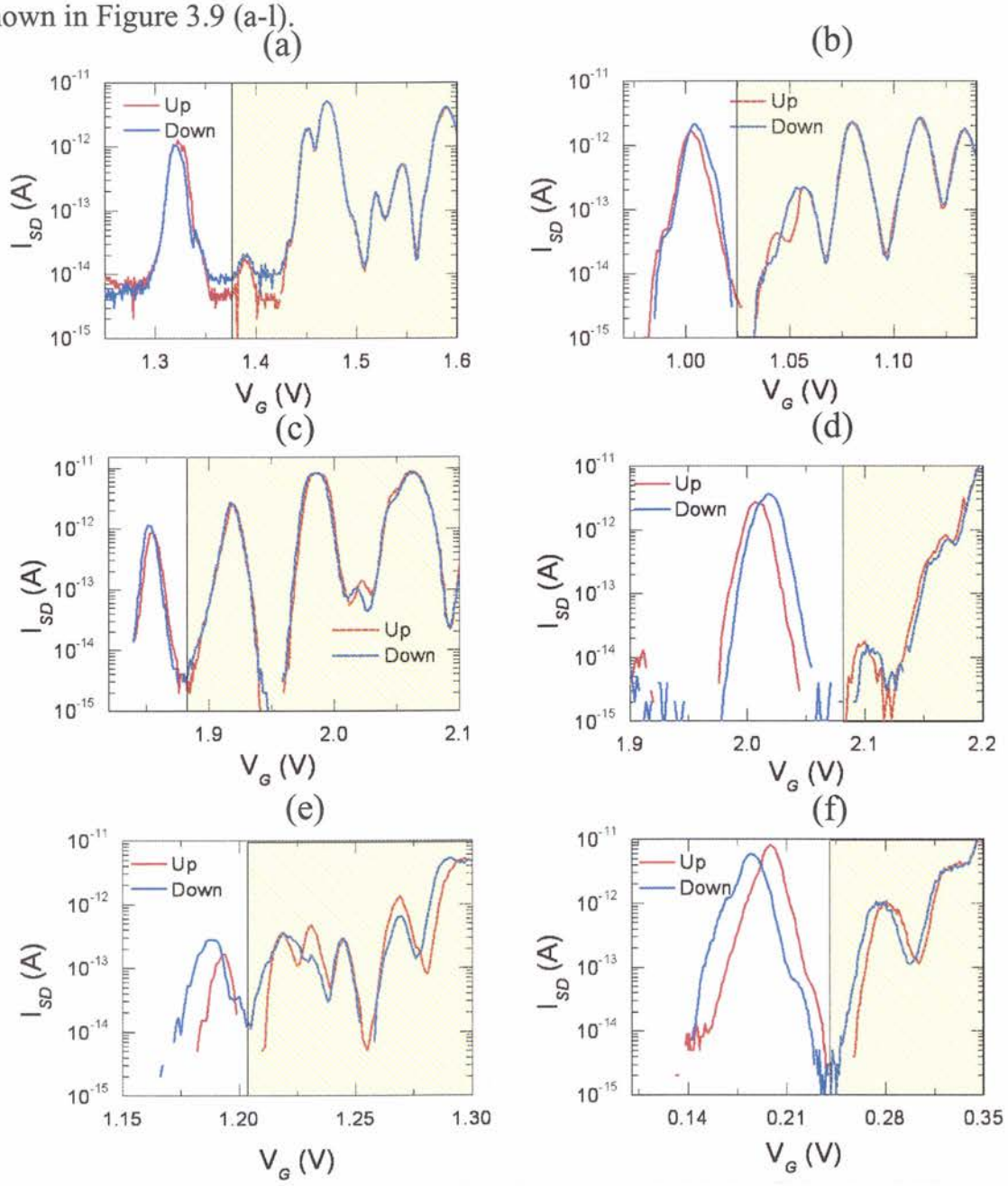
Typically, for the measurements discussed in this chapter, the temperature was set to 13~15 K. For all measurements, the substrate was grounded, while voltage V_G was applied to the Al top electrode. Source-drain bias was fixed at 5 mV. We fixed the measurement step to approximately 1mV/sec.

3.5.2 I_{SD}-V_G characteristics

We observed I_{SD}-V_G characteristics of our devices, as shown in Figure 3.9 (a-l). We measured around 40 devices. At low temperature, all the devices contain such current oscillations due to Coulomb blockade in the dopant-QDs [24]. We measured upward (increasing V_G) and downward (decreasing V_G) sweep for observing charging effects. Most of the devices contain some displacement in voltage between upward sweep and downward sweep curves. This voltage

displacement is a signature of charging.

However, this effect is most prominent at the first peak, and I will discuss this point more in Section 3.5.4. In our experiment, we mainly focus on the first peak, that is why I only highlighted first peak (outside of the yellow pattern), as shown in Figure 3.9 (a-l).



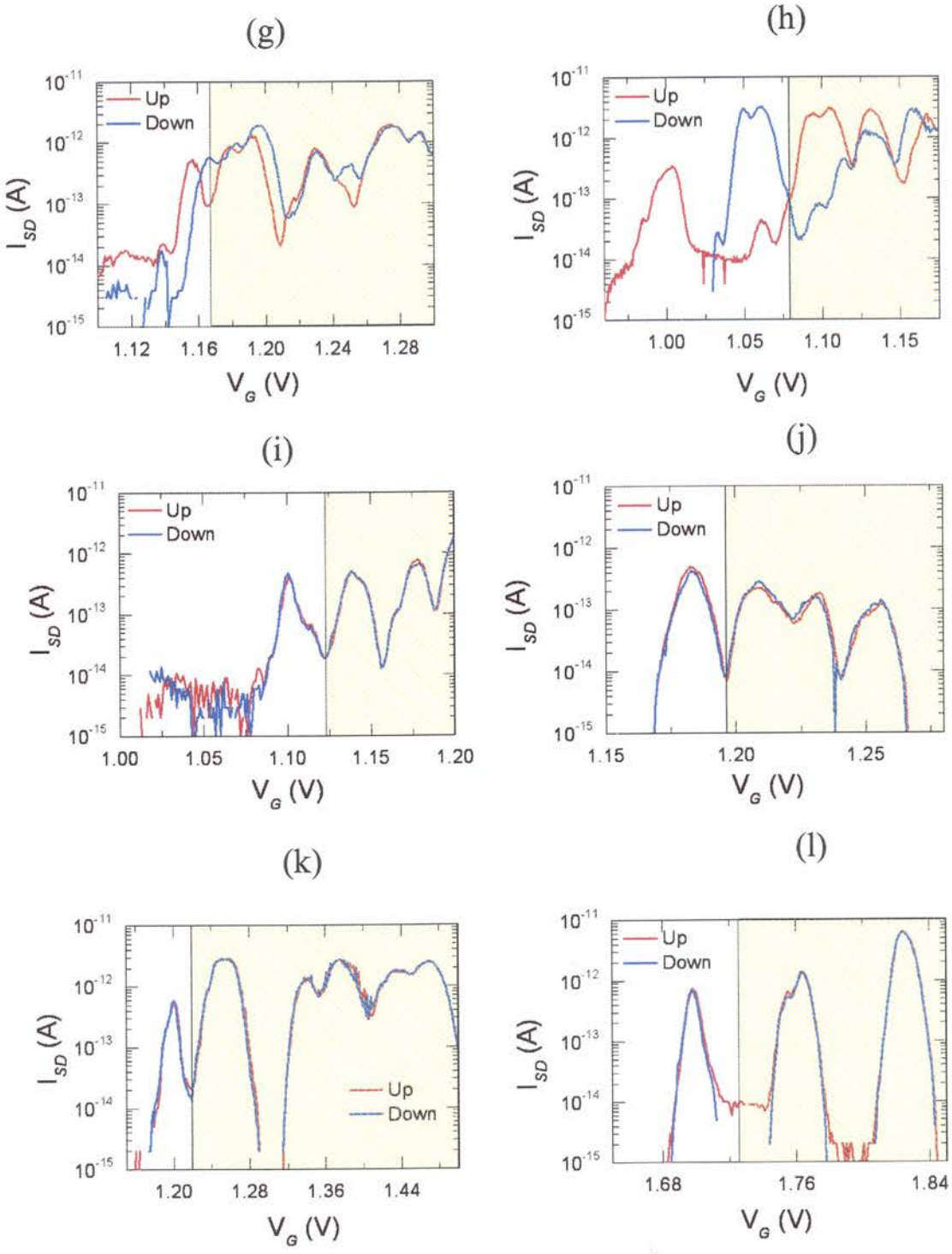


Fig.3. 9 I_{SD}-V_{FG} characteristics of a few devices exhibiting typical Coulomb oscillations (upward and downward V_G sweep).

The above I_{SD}-V_G characteristics can be categorized depending on their charging characteristics. From the above I_{SD}-V_G characteristics, we can observe different that types of charging effect appear, such as charging on the current peak or charging off the current peak and even for some of the devices no charging occurs at all. Therefore, I classified these charging characteristics into three categories.

1. Charging on the current peak.
2. Charging off the current peak.
3. No charging effect on the peak.

1. Charging on the current peak

This is most likely a charging effect caused by a single donor. The characteristics were measured for a limited V_G range around the first current peak. V_G was swept upward and, successively, downward with a sweep rate of 1 mV/s. In Figure 3.10 (a), abrupt current jumps can be observed on the first peak: a jump up in the upward sweep, at V_G = 1.345 V, followed by a jump down in the downward sweep, at V_G = 1.335 V. These features produce a fine but reproducible hysteresis, which can be ascribed to trapping and detrapping of a single electron in a memory dot. How these trapping and detrapping events happen in our devices is shown schematically in Figure 3.10 (b). An electron transfers from source to drain via

donor *D1*. By continuously increasing V_G, an electron can be shuttled to the trap donor *D2* and this change of the charge state will affect, at its turn, the single-electron conduction current. Similarly, if V_G is successively decreased, the electron should be eventually released from the trap as shown in Figure 3.10 (c). In case of event #1 electron is transfer from donor *D1* to *D2* and vice-versa for event #2.

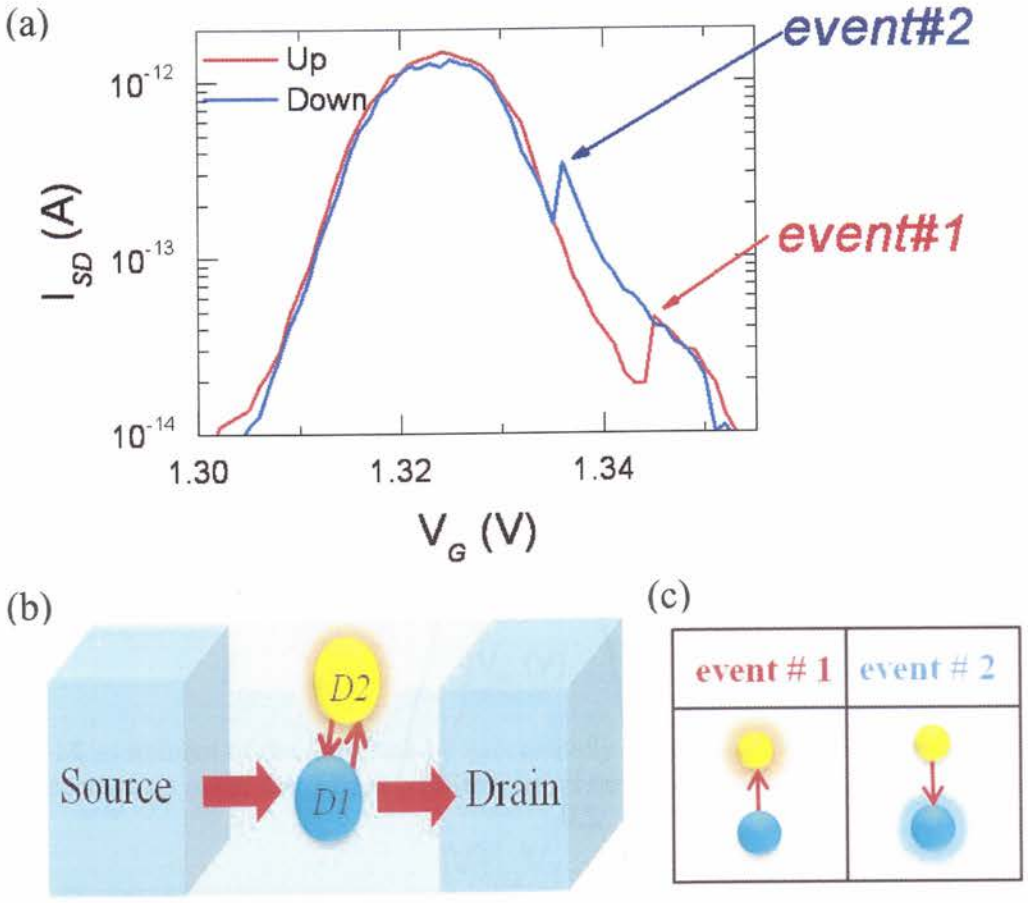


Fig.3. 10 (a) Measurement of the first peak by successively sweeping V_G upward and downward. Charging appear on the peak at V_G = 1.345V and discharging appear at V_G = 1.335 V which causes voltage shift. **(b)** Schematic view of single electron transfer between two donors *D1* and *D2*. **(c)** Event table shows electron transfer from donor *D1* to *D2* in case of *event 1* and *D2* to *D1* in case of *event 2*.

2. Charging off the current peak

In our observation we also observed charging effect off the current peak. Current jumps cannot be observed on the peak, but charging is evident from the displacement between the upward and downward curves, as shown in Figure 3.11. By applying positive gate voltage, an electron is transferred to the donor and conduction starts through the minimum donor potential, resulting in the first observable current peak. The first peak is separated by a Coulomb blockade effect from others peak. An electron exists to donor *D1* in the Coulomb blockade region after the first peak, so it may transfer to the nearest second donor by gradually increasing gate voltage, even though there is no current flow from source to drain.

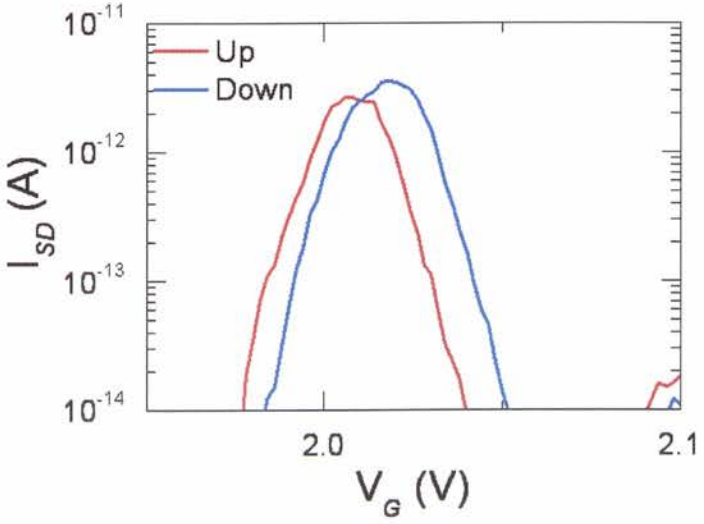


Fig.3. 11 Measurement of the first peak by successively sweeping V_G upward and downward. Charging appears off the current peak, in the zero current regions which causes voltage shift.

3. No charging effect on the peak

In principle, monitoring the first current peak allows us to evaluate single-electron tunneling via donor-QDs in the absence of other electrons in the channel. The distribution of donors in the channel differs significantly from device to device in our samples. In some devices, the lowest-potential donor can be detached from satellite donors of comparable potential, which would not allow electron shuttling between the two donors. As a result, no charging effect appears, which is illustrated in the example shown in Figure 3.12.

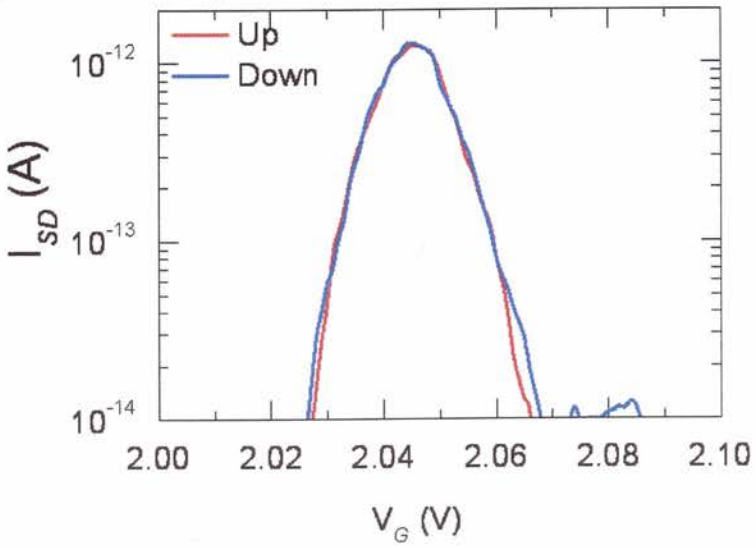


Fig.3. 12 Measurement of the first peak by successively sweeping V_G upward and downward. No charging appears on or off the current peak as a result no voltage shift.

5.3 Device statistics

As we can see in Figure 3.13, voltage distortion (ΔV_G) effect appears in most of our devices. From a number of about 40 devices measured, 85% exhibit hysteresis, while only 15% show a perfect match between up and down ramping

curves. In agreement with our consideration, nanowires containing many dopants are indeed appropriate for observing changing effect.

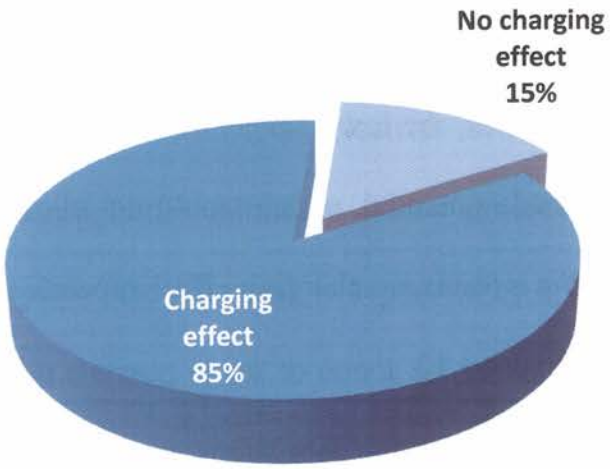


Fig.3. 13 Statistics of the device characteristics.

3.5.4 Importance of hysteresis on the first peak

The first peak corresponds to the initial stage of conduction in our devices. In my devices, containing more than one dopant, the overall potential landscape is modulated by the superposed potentials of all ionized dopants [13], [16], [68]. For nanostructures doped with phosphorus (P), the global minimum electronic potential will be formed close to the channel center as a consequence of the long-range potentials of the entire set of dopants, as shown schematically in Figure 3.14 (a). The potential of the dopant can be controlled by the gate voltage V_G. So, when the dopant potential is higher than the source Fermi level, electrons cannot travel, as a

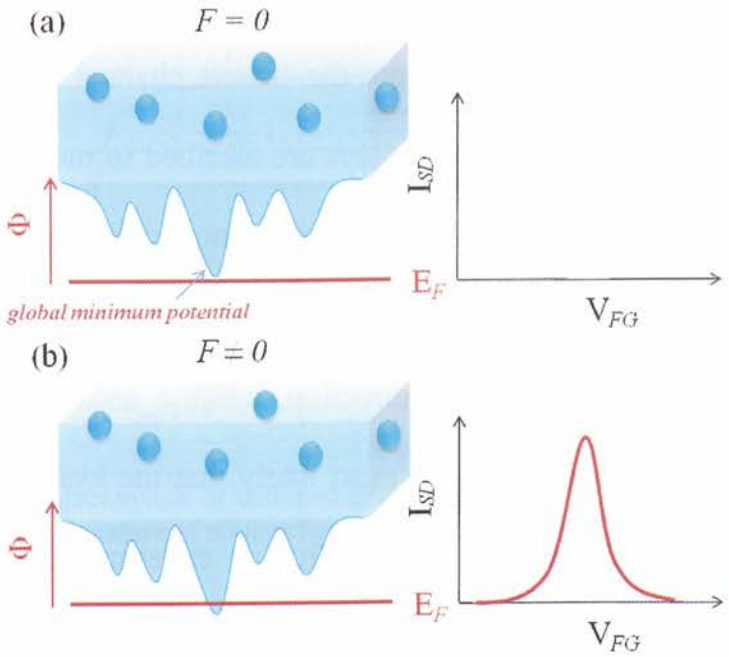


Fig.3. 14 (a) Dopant potential is higher than the source Fermi level, electron cannot travel, as a result no current peak can be observed. **(b)** Due to application of more positive gate voltage, global minimum potential is shifted to cross to the Fermi level and conduction start.

result no current peak appeared. When the channel minimum dopant potential is shifted close to the source Fermi level by more positive gate voltage, transport occurs through the dopant-induced QDs and the first current peak appears, as shown in Figure 3.14 (b). At even more positive V_G, electron is trapped in the dopant. Because the system is extremely small, one electron strongly increases the potential. Therefore, again no electrons can travel, which is in fact the Coulomb blockade regime. Figure 3.15 shows an electronic potential landscape, simulated for a random arrangement of donors. In these simulations, the channel is assumed to be depleted, so the potential is given by the superposition of the Coulomb potentials of

all ionized donors [13], [16], [68]. This situation corresponds to the onset of conduction, when the gate voltage aligns the lowest channel potential with the source Fermi level. The fine potential valleys are ascribed to individual donors. In some cases, we encounter the situation when two donors mainly dominate electron transport at this initial stage, as schematically shown: one donor (D_1) is the steppingstone for conduction in the x direction, while a second donor (D_2) may work as a single-electron trap. So, it is most likely that the hysteresis on the first peak appears due to such a dopant trap. In our experiment, we exclude the possibility of an interface trap being responsible for such effects. Furthermore, for confirmation, we measured un-doped devices, as shown in Figure 3.16. There are no hysteresis features appearing due to interface trap or others defects.

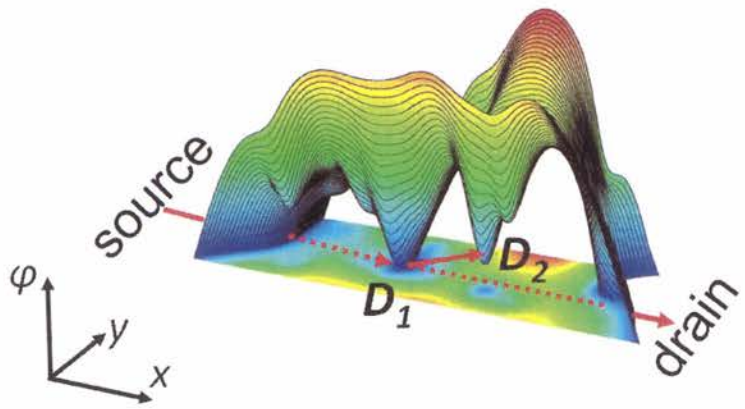


Fig.3. 15 Potential profile simulated for a random distribution of ionized dopants; two neighboring dopants are indicated. One donor (*D1*) work as a stepping stone of current path and the other donor (*D2*) work as a trap.

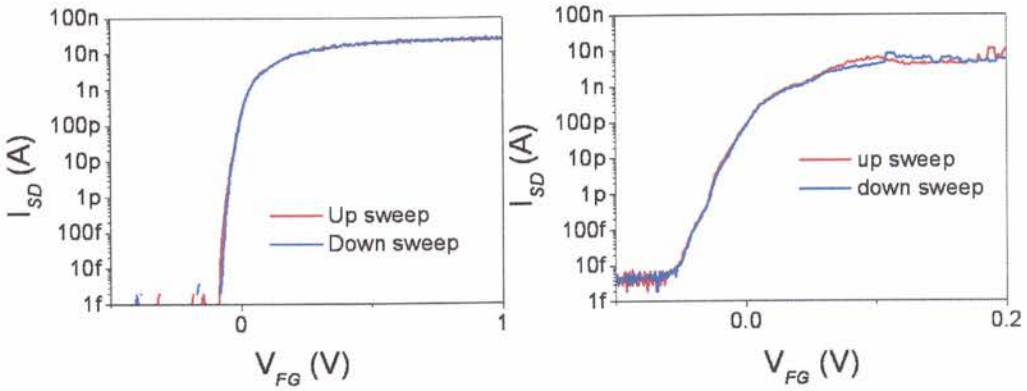


Fig.3. 16 I_{SD}-V_{FG} characteristics of undoped devices. There are no voltage distortion between up and down sweep is a signature of no interface trap occurred.

3.5.5 I_{SD}-time measurement

We have investigated a large number of devices in order to evaluate single-electron charging and discharging behavior. We typically measured I_{SD}–V_G characteristics for a V_G range surrounding the first peak, while sweeping V_G consecutively upward and downward, as indicated in Figure 3.17 (a). The V_G range is typically about 100 mV, while the current peak width is about 50 mV in width on average. We found devices that exhibit a hysteresis (shift) between the upward- and downward-ramping curves, indicating that charging occurred during voltage scan. The device characteristics shown in Figure 3.17 (a) (left) exhibit sudden current jumps and a partial shift of the curves for a small range of V_G (4~10 mV).

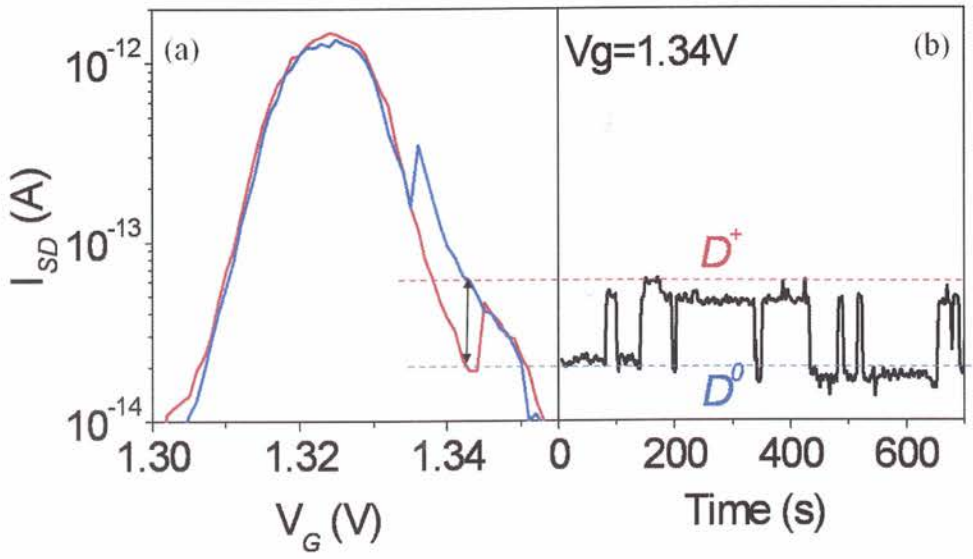


Fig.3. 17 (a) I_{SD}-V_G characteristics of the first peak (b) I_{SD}-time corresponds to the first peak. These jumps are indications of single-electron trapping and detrapping events.

When V_G is fixed within the hysteresis range and time evolution of the current is monitored, as shown in the right-hand Figure 3.17 (b), we can observe a random telegraph signal (RTS) with mainly two levels. This indicates a two-state trap, which suggests the possibility of a donor (ionized D^0 or neutralized D^+) being responsible for the current switching.

3.6 Conclusion

$I_{SD} - V_G$ characteristics presented here illustrate thus charging and discharging in a two-donor system. One donor works as a steppingstone in the conduction path, giving rise to the first current peak. Another donor modulates the current by trapping and detrapping one electron. This second donor does not contribute as a

conduction path, since we only observe a simple shift of the original peak after the current jump. Therefore, this trap donor is disconnected from at least one of the source and drain terminals. The shift of the current peak is most likely dependent on the initial charge state of the second donor. When an electron is stored into the second donor, it is working as an additional negative charge, which causes the peak to shift to the right. In our observation, 80% of the $I_{SD} - V_G$ characteristics show current peak shift to the right due to electron trap in a phosphorus dopant. Some of the characteristics exhibit also shifts to the left, most likely due to an effective positive charge appearing in the downward sweep. Although the origin is not clear at this moment, such a positive charge may be due to the ionization of a phosphorus dopant which was initially under freeze-out condition, i.e., neutral. Furthermore, the charging occurs typically on the current peak, which indicates that conduction through the first donor and trapping in the second donor are correlated. This is a strong indication that trapping and detrapping occurs by single-electron transfer between the two donors. Other mechanisms, such as injection from one terminal, although unlikely in our system, may also be taken into consideration.

Chapter 4
Theoretical approach for double donor system
4.1 Monte-Carlo simulation based on Coulomb blockade theory

Single-electron transistors contain one or more small conductive regions (so-called Coulomb islands or quantum dots), weakly coupled to each other and leads through tunnel junctions. These devices operate on the basis of single-electron tunneling and the Coulomb blockade effect that occurs when electrons localized on the islands block the current flow for a significant range of applied voltages. We used a Monte Carlo (MC) simulation developed on the basis of the Coulomb blockade orthodox theory in our study of single-electron transfer [36], [69], [70], [71]. According to this theory, forward and reverse tunneling rates of electrons across a specific junction are given by:

$$\Gamma^{\pm} = \frac{1}{e^2 R_j} \frac{\Delta F^{\pm}}{\left[1-\exp\left(-\frac{\Delta F^{\pm}}{K_B T}\right)\right]} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where e is the elementary charge and $\Delta F^{\pm}$ is the change in system free energy owing to forward or reverse tunneling events. Free energy is calculated as the sum of the total electrostatic energy of the system and the work performed by external sources. Equation (1) simplifies for T = 0, K in the following form:

$$\Gamma^{\pm} = \begin{cases} 0 & (\Delta F^{\pm} < 0) \\ \dfrac{\Delta F^{\pm}}{e^2 R_j} & (\Delta F^{\pm} > 0) \end{cases} \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

As also described by eq. (2), tunneling events are allowed only if they lower the free energy of the entire system. The average interval between successive tunneling events estimated from eq. (2) is $1/\Gamma^{\pm}$. In our simulation, we use tunneling intervals $u^{\pm}$ that incorporate a random number r ($0 < r < 1$) in the calculation to reflect the stochastic nature of tunneling events, as shown in the following equation:

$$u^{\pm} = \frac{1}{\Gamma^{\pm}} \ln\left(\frac{1}{r}\right) \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

For all tunnel junctions, we calculate $u^{\pm}$ values and choose a tunneling event with the minimum $u^{\pm}$, which is regarded as the tunneling event that actually occurred. We then repeat the same procedure for the next events starting at $t = u^{\pm}$.

4.2 Modeling and Equivalent circuit for double donor system

4.2.1 Fixed-parameter two dot circuit

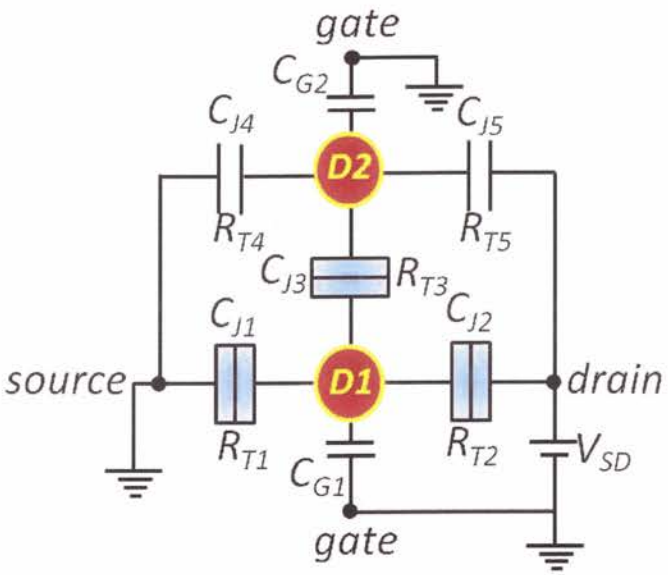


Fig.4. 1 Equivalent circuit for fixed-parameter two dot system.

As I already explained from the experimental results, only two donors can produce a charging effect by transfer of a single electron from the conduction donor *D1* to the nearest donor *D2* in our system. We used Coulomb blockade Monte Carlo simulation to prove this charging phenomenon for a simple 2-dot circuit, considering two donors *D1* and *D2,* as shown in Figure 4.1. In this circuit, donor *D1* dominates the carrier transport and donor *D2* represents the dot adjacent to the path, whose charging state influences the tunneling transport. Charging of the adjacent dot occurs through the tunnel junction $C_{J3}R_{T3}$. We intentionally disconnected the arm resistances R_{T4} and R_{T5} of the adjacent donor *D2* to avoid the

electron tunneling from source or drain to this adjacent donor *D2*.

We used symmetric parameters, such as gate capacitances $C_{G1} = C_{G2} =$ 0.01 aF, junction capacitances C_{J1}, C_{J2}, C_{J3}, C_{J4}, $C_{J5} = 4$ aF, tunneling resistances R_{T1}, R_{T2}, $R_{T3} = 1$ GΩ. From simulation results, we obtained the hysteresis which is due to trapping and detrapping at the gate voltages 1.6 V and 0 V, respectively, as shown in Figure 4.2. The trapping/detrapping mechanism can be explained by calculation of system free energy, which will be explained in the next section.

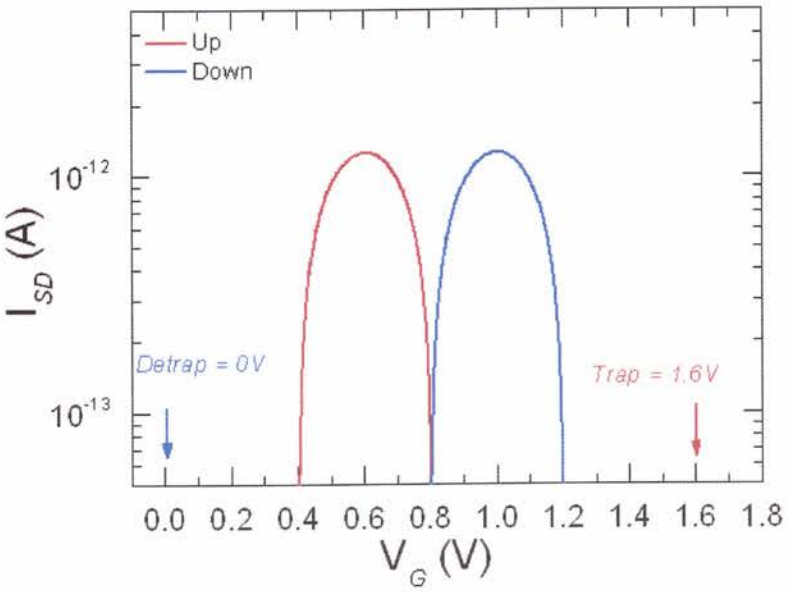


Fig.4. 2 I_{SD}-V_G characteristics of fixed-parameter two dots circuit.

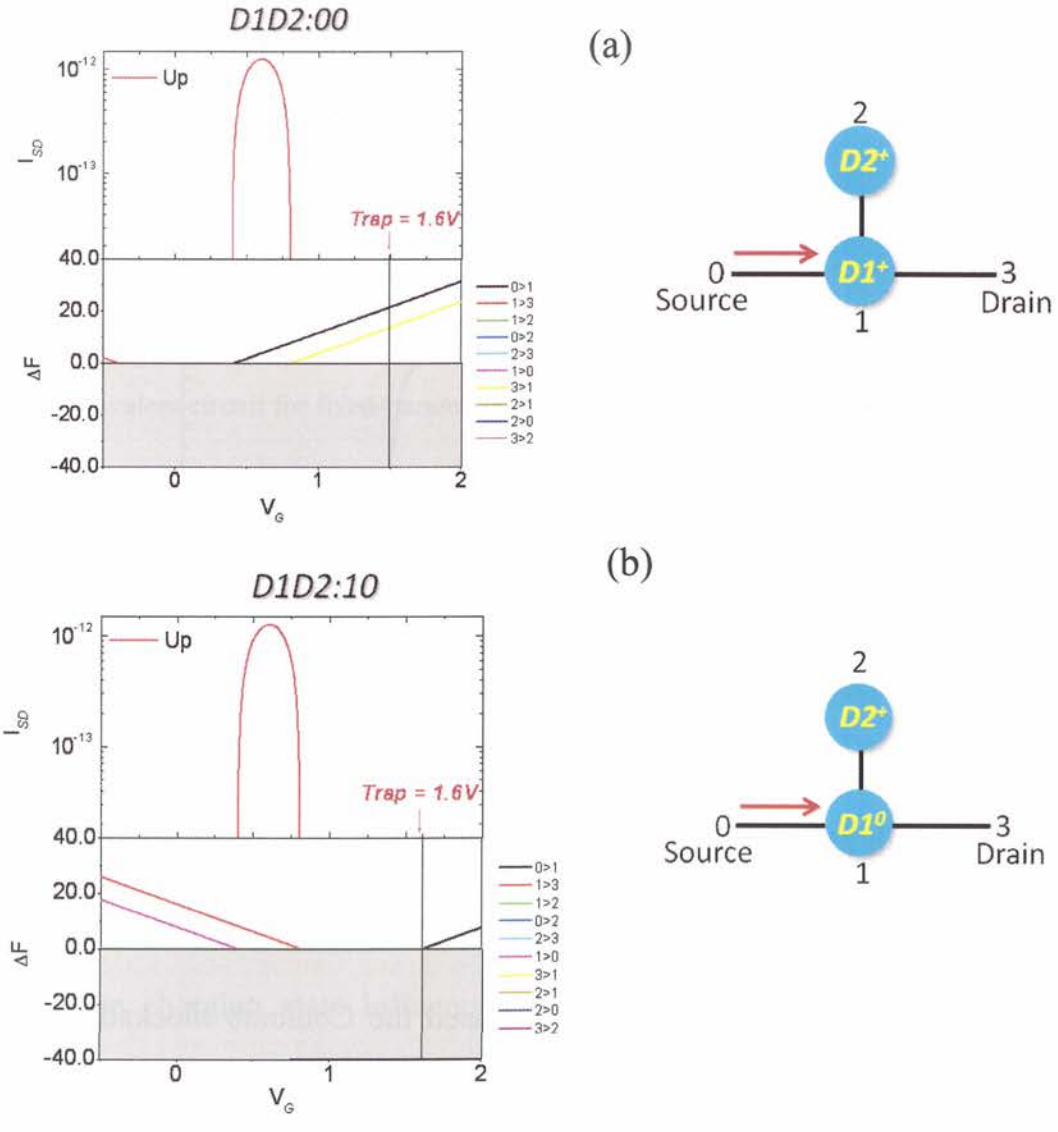
4.2.2 System free energy calculation

Regarding the calculation method, I used the Coulomb blockade orthodox theory in my study of single-electron transfer, as explained in the previous Section 4.1. Free energy is calculated as the sum of the total electrostatic energy of the

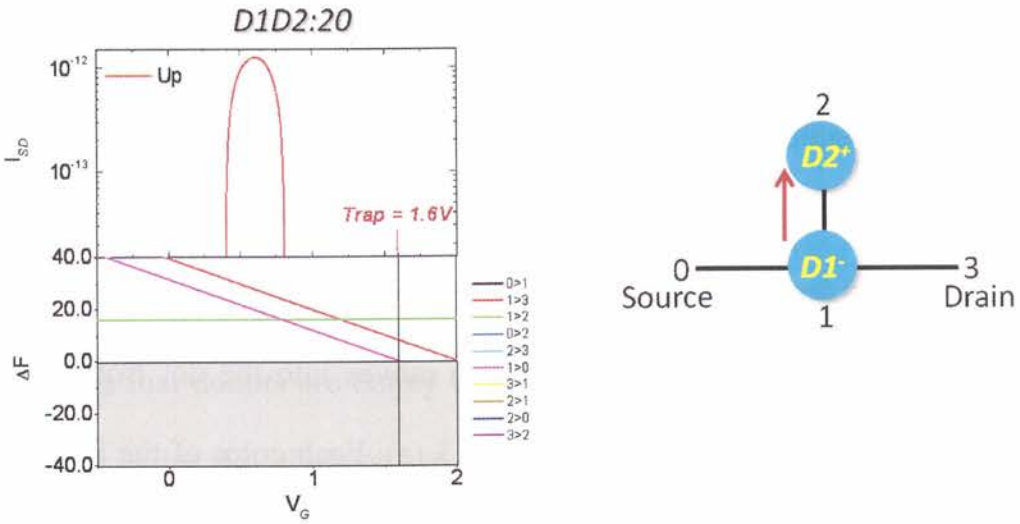
system and the work performed by external sources.

We considered fixed-parameter two dot circuit, as show in Figure 4.1 for our calculation. Based on system free energy calculation, we can understand the electron trap and detrap mechanism, which will be explained in the following:

Trap mechanism V_G = 1.6 V



(c)



(d)

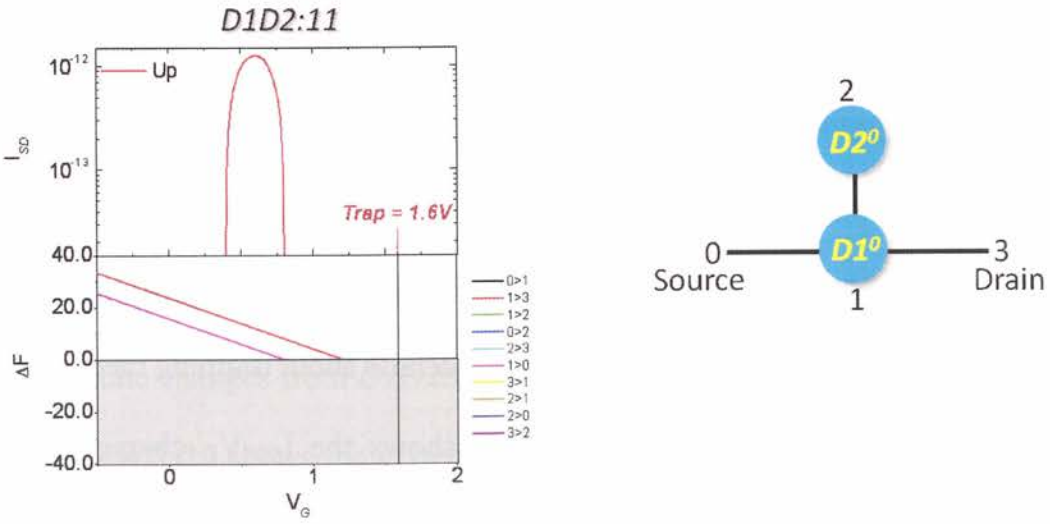


Fig.4. 3 (a-d) Trap mechanism for fixed two dot systems. Left-hand upper figure show I_{SD}-V_G characteristics for which trapping occurred at V_G= 1.6V. Left-hand lower figure shows the system free energy calculation corresponding to upper I_{SD}-V_G. Right-hand schematic view shows the charge state for the fixed-parameter two dot system.

System free energy calculations allow us to know how trapping and detrapping occurred in our fixed-gate capacitance two dot system. Figure 4.3 (a) left-hand lower figure shows the system free energy calculation corresponding to the upper I_{SD}-V_G characteristics. The inclined line is defining the electron movement from source/drain to the dot or from dot to source/drain. If the inclined line directions are rightward down to up, it means that electron moves into the dot from source or drain, as shown by the black line in Figure 4.3 (a). Each color of the inclined line indicates an event of electron transfer. For example, black and yellow inclined lines correspond to events 0 > 1 and 3 > 1, respectively. However, as the arm resistance of our circuit (R_{T4} and R_{T5}) is significantly high to prevent electron transfer from source or drain to the dot 2, I will purposely avoid showing four events, namely 0 > 2, 2 > 0, 3 > 2, 2 > 3. In case of inter-dot electron transfer (events 1 > 2 and 2 > 1), we observed a horizontal line due to the symmetry of the system, as shown in Figure 4.3 (c). In the following, I will explain details about trapping mechanism.

Figure 4.3 (a) left-hand upper figure shows the I_{SD}-V_G characteristics for fixed-parameter 2 dot circuit, as also explained in the previous Section 4.2.1. When the voltage is swept up from low to high, trapping occurs at a gate voltage V_G = 1.6 V. As trapping happens in the zero current regions, we cannot observe the charging on the current peak.

Left-hand lower figure shows the system free energy with respect to gate

voltage (Δ F-V_G) characteristic. Left-hand upper I_{SD}-V_G and lower Δ F-V_G correspond to each other. In Figure 4.3 (a), trapping voltage V_G = 1.6V is marked by a solid line along with the free energy graph to understand the energetic transfer of an electron on those critical gate voltages.

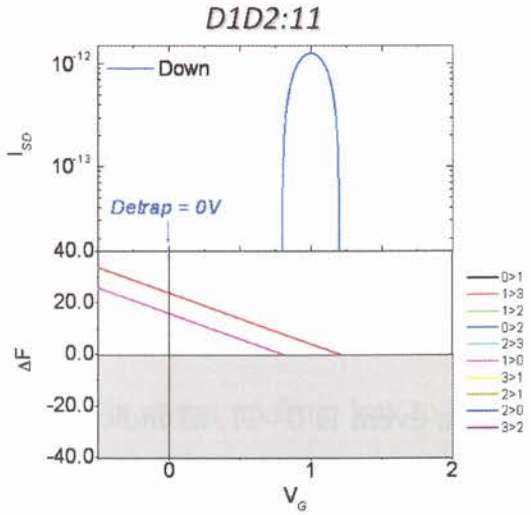
At the beginning, we consider the charge state for two donors, *D1D2:00*, which means that donors are empty of electrons. Donors *D1* and *D2* are thus both ionized, and under this situation we calculate the system free energy. The system free energy for (00) charge state shows that the favorable event is 0 > 1 (black down to up inclined line), which means that one electron is favorable to transfer from source to *D1*, as schematically shown in the right-hand figure, where donors *D1* and *D2* are ionized (D^+). The current peak is mainly dominated by the sequential events 0 > 1 and 1 > 3, that is why free energy calculation graph shows 0 > 1 event is just corresponding to the starting of the current peak. After event 0 > 1, the charge state changes from *D1D2:00* to *D1D2:10.*

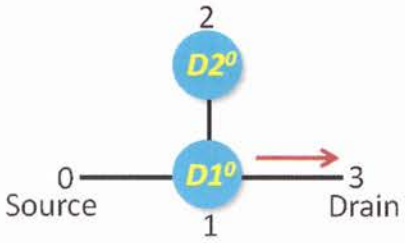
Figure 4.3 (b) shows the system free energy for donor charge state *D1D2:10,* which means that one electron is located in *D1* while *D2* is empty of electron. At the trapping gate voltage V_G = 1.6 V, favorable event is 0 > 1, as indicated by the black inclined line down to up. It means that one more electron is favorable to transfer to *D1* from source, even though one electron is already located there. Then, the system charge state becomes *D1D2:20.*

Figure 4.3 (c) shows the system free energy for donor charge state *D1D2:20.* The event 1 > 2 is now favorable for all the gate voltage range, including the trapping voltage V_G = 1.6 V. Now, one electron will transfer from donor *D1* to donor *D2* and trapping occurs. Then, the system charge state becomes *D1D2:11*, as shown in Figure 4.3 (d). We can also explain the detrapping mechanism at V_G = 0 V by following similar system free energy calculation. Now, I will explain details about detrapping mechanism is, as follows.

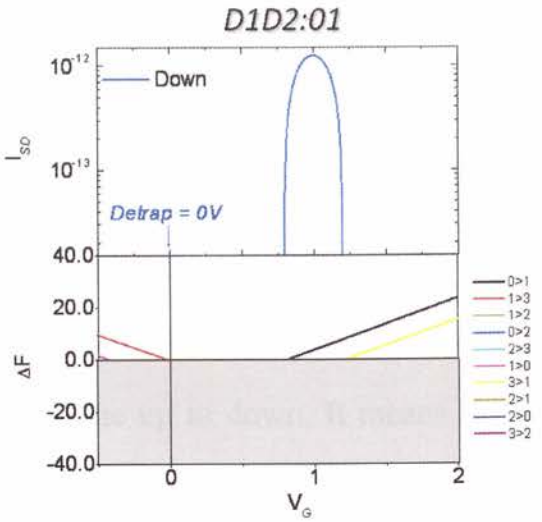
Detrap mechanism V_G = 0 V

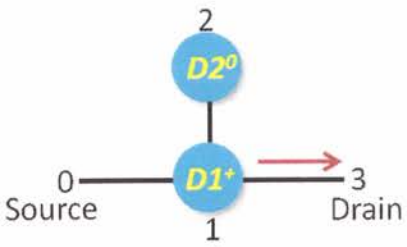
(a)



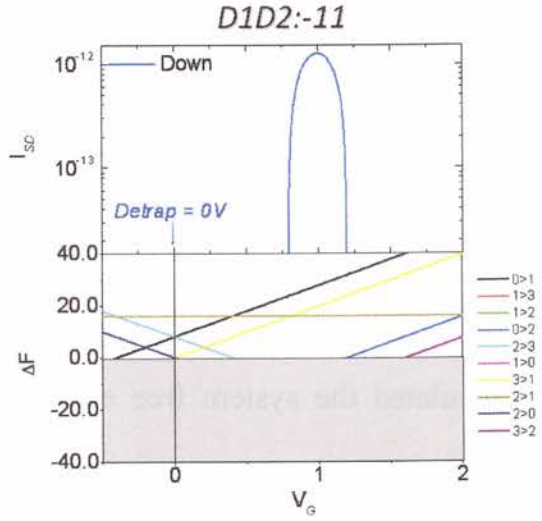


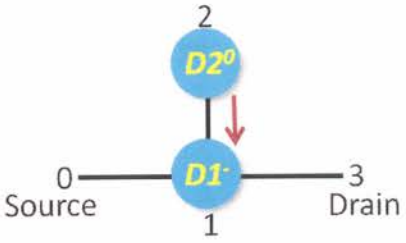
(b)


D1D2:01
Down
Detrap = 0V
I_{SD}
10^{-12}
10^{-13}
40.0
20.0
0.0
-20.0
-40.0
ΔF
0
1
2
V_G
0>1
1>3
1>2
0>2
2>3
1>0
3>1
2>1
2>0
3>2


2
$D2^0$
0
Source
$D1^+$
3
Drain
1

(c)


D1D2:-11
Down
Detrap = 0V
I_{SD}
10^{-12}
10^{-13}
40.0
20.0
0.0
-20.0
-40.0
ΔF
0
1
2
V_G
0>1
1>3
1>2
0>2
2>3
1>0
3>1
2>1
2>0
3>2


2
$D2^0$
0
Source
$D1^-$
3
Drain
1

(d)

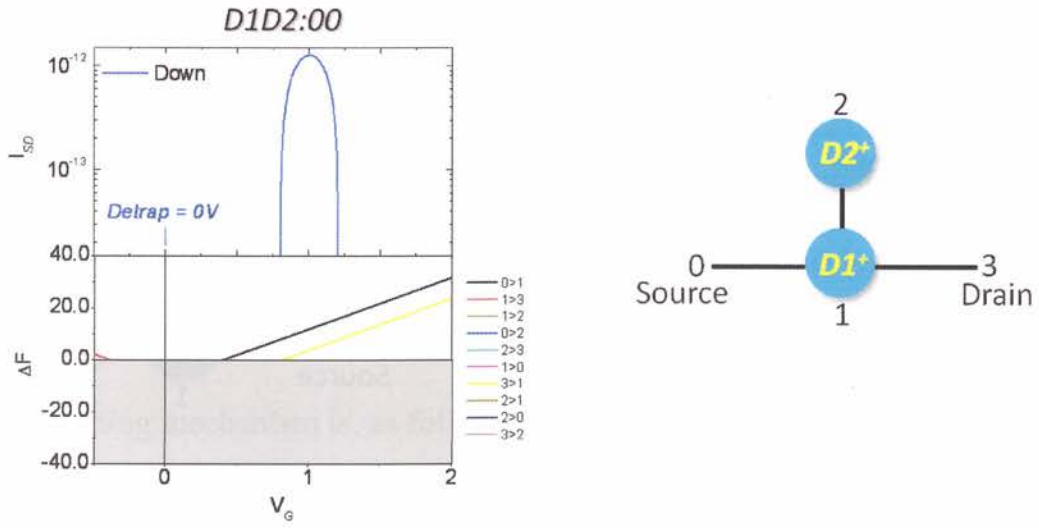


Fig.4. 4 (a-d) Detrapping mechanism for fixed-parameter two dot systems. Left-hand upper figure show I_{SD}-V_G characteristics where detrapping occurred at $V_G = 0V$. Left-hand lower figure shows the system free energy calculation corresponding to the upper I_{SD}-V_G. Right-hand schematic view shows the charge state for two dot system.

Figure 4.4 (a) left-hand upper figure shows I_{SD}-V_G characteristics for fixed-parameter 2 dot circuit. When the voltage is swept down from high to low, detrapping occurs at a gate voltage $V_G = 0$ V. For the higher gate voltage region, the charge state is *D1D2:11*, which means that donors *D1* and *D2* both contain one electron, and under these conditions we calculated the system free energy. The system free energy for *D1D2:11* charge state shows that the favorable event is 1 > 3 (red up to down inclined line), which means that one electron is favorable to transfer from *D1* to drain, as schematically shown in the right-hand figure. It is

reasonable that the current peak is mainly dominated by the sequential events 1 > 3 and 0 > 1, that is why free energy calculation graph shows 1 > 3 event is again just corresponding to the starting of the current peak. The charge state will change thus from *D1D2:11* to *D1D2:01.*

Figure 4.4 (b) shows the system free energy for donor charge state *D1D2:01,* which means that donor *D1* is empty of electron and *D2* contains one electron. At the gate voltage V_G = 0 V, the favorable event is 1 > 3, as indicated by the red inclined line up to down. It means that one more electron is favorable to transfer out from *D1* to drain. Then the system charge states become *D1D2:-11.*

Figure 4.4 (c) shows the system free energy for donor charge state *D1D2:-11.*The event 2 > 1 is now favorable for all the gate voltage ranges, including the detrap voltage V_G = 0 V. Now one electron will transfer from donor *D2* to donor *D1* and detrapping occurs. Now, the system charge states become *D1D2:00*, as shown in Figure 4.4 (d).

Discussion

Above, I showed that the trapping and detrapping mechanisms can be understood by system free energy calculations. In case of fixed-gate capacitance two-dot simulation, electron trapping and detrapping both events required double-electron charge occupancy, as can be understood from the schematic view shown in Figure 4.5 (a)-(b).

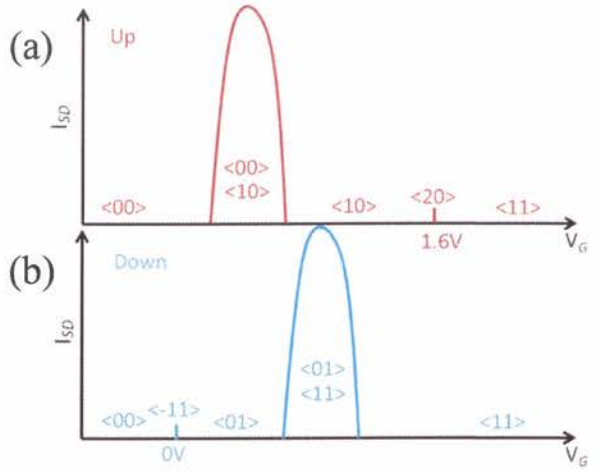


Fig.4. 5 (a) Schematic I_{SD}-V_G characteristics of fixed-gate capacitance two-dot circuit showing the charge states for up-ramping. Trapping occurred at V_G = 1.6 V. **(b)** Schematic I_{SD}-V_G characteristics of fixed-gate capacitance two-dot circuit showing the charge states for down-ramping. Detrapping occurred at V_G = 0 V.

From the above schematic I_{SD}-V_G characteristics, we can see the charge state for the full V_G range. Figure 4.5 (a) shows that, at the beginning of the gate voltage range, the charge state is <00>. By increasing V_G, the current peak appears by incorporating <00> and <10> charge states. At V_G = 1.6 V, we observed the charge

state <20> and then immediately the charge state changes to <11>. Finally, the charge state <11> remains until the end of the V_G range. Therefore, the system is mainly stable with <00>, <10>, and <11> charge states, at different V_G's. When the system is expected to become <01> by 1 > 2 event after <10>, by increasing V_G it was followed by a short unstable transition <20> by 0 > 1 event, and then finally it changes to <11> stable charge state. It means that one electron can switch energetically in case of fixed-gate capacitance two-dot system, but two electrons must be allowed to enter one dot, i.e., <20> charge state configuration is involved. In the same way, for detrapping mechanism, we found that the charge state follows <11>, <01>, <-11>, and <00>. Double-charge occupancy is mandatory for detrapping also at V_G = 0 V, as shown in Figure 4.5 (b).

Previous studies on conventional two-dot circuits do not explicitly clarify the number of electron occupancy in the memory dot. However, it is most likely that more than one electron is accommodated in the trap dot. We also explained the stability diagram for fixed two dot system to clarify the double-charge occupancy.

4.3 Stability diagram for fixed double dot system

In the previous sections, I showed schematically that the double-charge occupancy is necessary for energetic electron transfer between two donors. It would be more convenient to read the electron transfer process from the stability diagram

domains. It is also important to know how the electron transfer is influenced by the drain voltage, in other words, how does the conductivity modify with the bias voltage. For clarifying this, I simulated I_{SD}-V_G characteristics with different V_D's, as shown in Figure 4.6 (a).

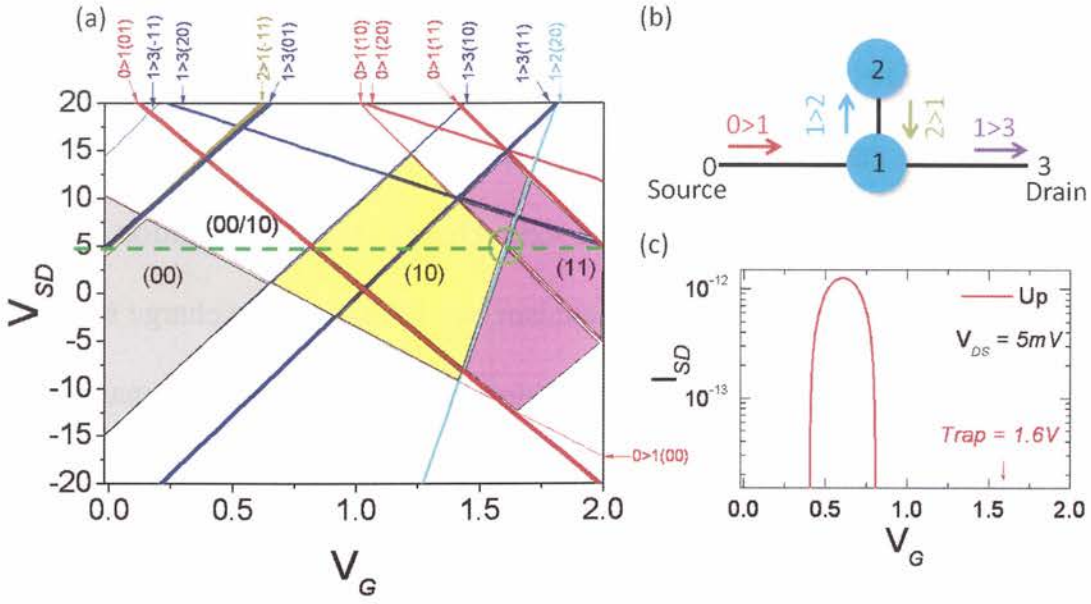


Fig.4. 6 (a) Simulated stability diagram for fixed two dot system. **(b)** Schematic two dot system, showing possible event for an electron transfer. **(c)** I_{SD}-V_G characteristics at V_{DS} = 5mV of fixed-gate capacitance two-dot circuit showing the charge states for up ramp.

Figure 4.6 (a) shows the stability diagram for fixed-parameter two dot system. Each differently-colored inclined line is corresponding to a different electron transfer event, as schematically shown in Figure 4.6 (b). For example, when electron moves from source to dot 1, that event is denoted as 0 > 1, which is the red inclined line. The left side region of the red line is unfavorable for an electron to

transfer. When electron moves out from the dot, corresponding to the blue inclined line, this is related to the 1 > 3 event. The right side region of the blue line is unfavorable for an electron to transfer. We also can see also that each of the lines has different thickness, which is a guide for the eyes to indicate different charge states.

If we consider the green dashed line, which corresponds to 5 mV, there is zero current from 0 V to 0.35 V, as shown by the light grey region. At V_G = 0.36 V, the electron is favorable to transfer. The first current peak appears within the range from 0.36 V to 0.81 V, as shown in Figure 4.6 (c). After V_G = 0.81 V, there is again a zero current region. This is the <10> Coulomb blockade, as shown by the yellow-colored region. At V_G = 1.6 V, we can see that there is a cross line between 0>1 and 1>2 events, marked by green circle, as shown in Figure 4.6 (a). It means that at the same voltage two events occur, at first one electron comes from source to dot 1, and the charge state become <20>, then at the same voltage one electron moves to dot 2 from dot 1, causing an electron trapping.

In conclusion, we observed the double-electron occupancy by studying also the stability diagrams. In the stability diagram shown in Figure 4.6 (a), two events appear at the same voltage, as marked by green circles. The cross point is a short transition period for an electron, before becoming a stable condition, which is indicated by the pink-colored <11> Coulomb blockade region.

We also simulated the stability diagram for downward sweep which will be explained in the next figure in combination with the upward sweep.

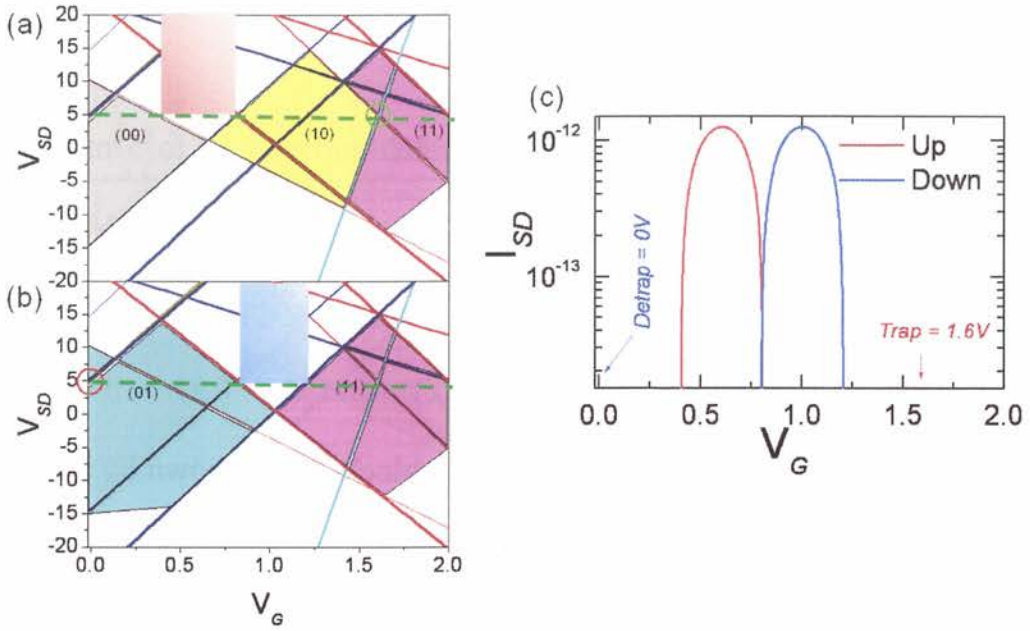


Fig.4. 7 **(a)** Simulated stability diagram for fixed-parameter two dot system. **(b)** Schematic two dot system, showing possible events for an electron transfer. **(c)** I_{SD}-V_G characteristics at V_{DS} = 5mV of fixed-gate capacitance two-dot circuit showing the charge states for up-ramping.

Figure 4.7 (a) shows the stability diagram for upward sweep, as I explained in the previous section. The current flow region is marked by red color, which corresponds to the first peak during upward sweep. Figure 4.7 (b) shows most importantly the stability diagram for the downward sweep. The current flow region is marked by the blue color, which is the first current peak during downward sweep. Detrapping occurs at $V_G = 0$ V, as show by the red circle. However, two sequential

events, 1>3, and 2>1, happen at $V_G = 0$ V.

We can conclude that energetic switching can be observed in case of fixed-parameter two dot system, but double-electron charge is necessary. Due to this kind of trapping and detrapping events, we were able to observe the full shift, as shown in Figure 4.7 (c).

Several essential points that must be considered when simulating two-donor circuits are indicated next:

1. New concept of donor-induced quantum dot requires limiting electron occupancy to only one electron per dot.
2. Variable donor-gate capacitance can provide a way to effectively limit the electron occupancy.
3. Although electrostatic conditions govern the electron charging voltages, kinetic conditions, represented by the tunneling junction resistances, also play an important role for obtaining hysteresis in a two-dot system.

4.4 Concept of variable donor gate capacitance in Si channel

4.4.1 Introduction

It is well known that the electrical and optical properties of bulk and low dimensional semiconductors strongly depend on the presence of donor impurities. Recently, there has been an enhanced interest to study shallow donor impurities near an interface, either with vacuum or at a metal-oxide semiconductor interface, because of its importance in atomic-scale electronics and nano-electronics. This is a

consequence of the growing tendency for miniaturization of electronic devices.

In the other limit of a dopant close to the gate dielectric, it is possible to adiabatically pull the donor-bound electron into the potential well formed at the interface [17], [72], [73]. Donors proximal to the interface provide an important mechanism for quantum functionality in a range of novel quantum device proposal. The hybridized donor-interface system was recently proposed as the basis for quantum control of electron states at the interface [18], [19], [72], [74], [75], [76], [77], [78], [79]. These theoretical and experimental studies of the hybridization of electron wave function between the donor's Coulomb well and interface well allows us to develop the theory of variable donor-gate capacitance in thin Si channel. Furthermore, from the viewpoint of our device geometry (gate surrounding 10-nm-thick Si channel), it is also obvious to assume that most of the donors near the interface are sensitive to the field and as a result the donor potential can be easily distorted by applying an electric field. In consequence, variable donor-gate capacitance should be considered, as described in the following.

4.4.2 Modeling a single donor near the interface

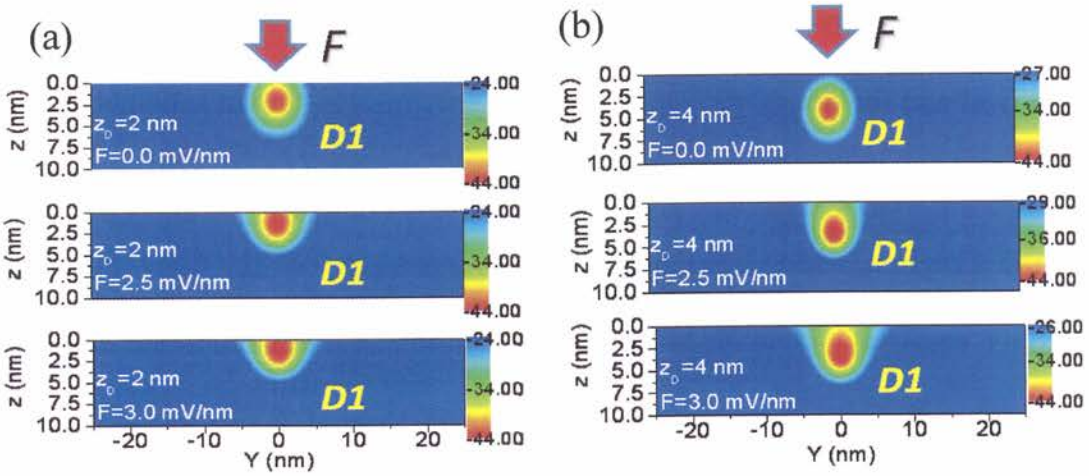


Fig.4. 8 (a) A single donor *D1* located 2nm away from Si/SiO_2 gated interface. By applying electric field $F = 0\sim3$ mV/nm the donor potential deviate towards interface. **(b)** A single donor *D1* located 4 nm away from the Si/SiO_2 interface. Donor potential is less sensitive to the electric field.

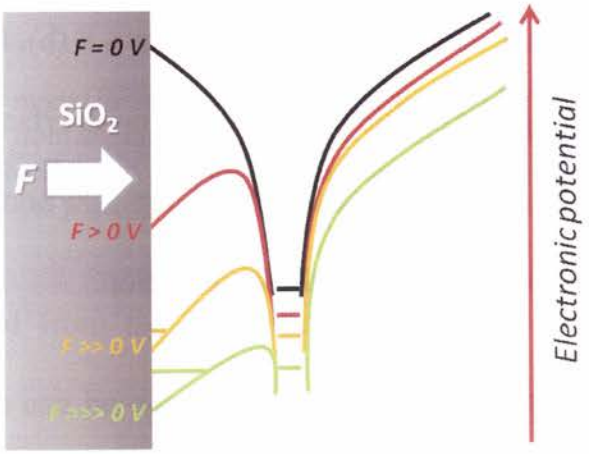


Fig.4. 9 A single donor potential extended towards the interface for different fields. At higher field value (light green state) the interface well and donor well are aligned in energy.

We consider initially a single donor *D1* in the thin Si channel (10 nm), located relatively close to the Si/SiO_2 interface. Figure 4.8 (a) shows *D1* is located 2 nm away from the interface. For zero field the electronic potential for donor *D1* suffers

almost no change. When we apply the electric field F = 2 and 3 mV/nm respectively, the electronic potential extended toward interface. At this stage, the interface well and the donor well are aligned in energies, as shown schematically in Figure 4.9.

In this regime, strong hybridization is observed between the donor states and the interface states, as the donor-bound electron tends to be ionized to the interface.

Figure 4.8 (b) shows the case when *D1* is located 4 nm away from the interface. As the donor position is relatively far compared to Figure 4.8 (a), the donor potential is less sensitive to the electric field, and as a result no significant change appears with higher fields, as shown in Figure 4.8 (b). However, more study is necessary to understand the physics of single donor-interface interactions. In my simulation, I mainly focus on the two-donor model in thin Si channel under electric field, which will be explained briefly in the next section.

4.4.3 Modeling of a double-donor system in Si channel

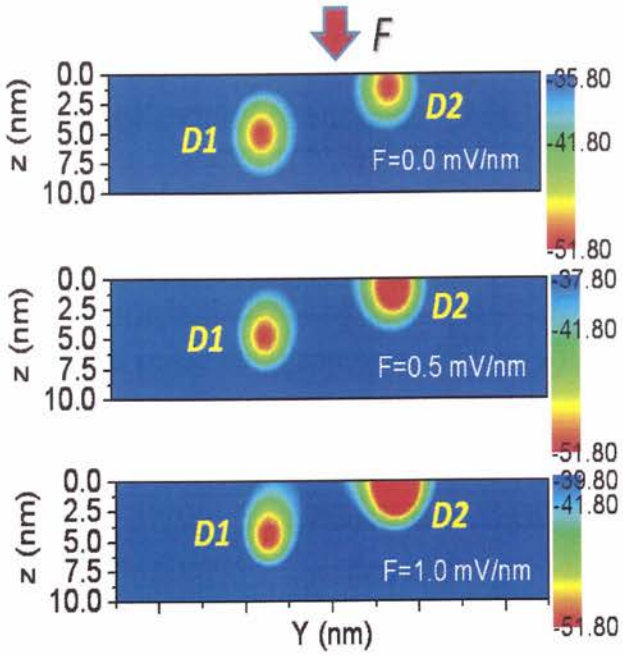


Fig.4. 10 Double-donor model in Si channel under electric field F = 0, 0.5, and 1 mV/nm. Donor *D1* located relatively far from the interface as a result donor potential is not influenced even for a high field. On the other hand donor potential *D2* influenced by the electric field as it is relatively close to the interface and the potential extended towards the surface.

As I explained from the experimental results, shown in Figure 3.10 (a), abrupt current jumps can be observed on the first peak: a jump up in the upward sweep, at V_G = 1.345 V, followed by a jump down in the downward sweep, at V_G = 1.335 V. These features produce a fine but reproducible hysteresis, which can be ascribed to one donor works as a steppingstone in the conduction path, giving rise to the first current peak. Another donor modulates the current by trapping and detrapping one electron.

In order to reproduce single-electron transfer characteristics in simulation, I

model two-donor system, as shown in Figure 4.10. Donors *D1* and *D2* are both located in the 10-nm-thick Si channel. *D2* resides close to the interface, while on the other hand *D1* is located away from the interface. So, by applying the electric field, the potential of donor *D2* is expanded effectively towards interface and as a consequence voltage-dependent donor-gate capacitance can be considered. At the same time, the potential of donor *D1* remains unchanged as it is less sensitive to the electric field, so the donor-gate capacitance will be fixed for this donor.

In addition, voltage-dependent donor-gate capacitance is very reasonable for donors in thin Si channels. Figure 4.10 shows the y-z cross-sectional potential landscape for a simplified arrangement of two donors in a thin Si channel. Three cases are shown: without and with an electric field F applied vertically (along z axis). Current flows in the x direction through donor *D1*. This donor, located relatively far from the interface (5 nm here), is not significantly affected by the electric field. On the other hand, the second donor, *D2*, is close to the interface (1 nm here). For such superficial donor, it is known that the potential expands at the interface under electric field [17], [44], [73], [80], [81]. The cross-sectional area towards the gate and, implicitly, the donor-gate capacitance (C_G) increases with electric field (i.e., voltage V_G). Therefore, for such a donor, C_G is continuously changing with V_G. In our simulation, for the first time, we consider variable donor-gate capacitance, in a procedure will be explain in details in the next section.

4.4.4 Equivalent circuit for variable donor-gate capacitance

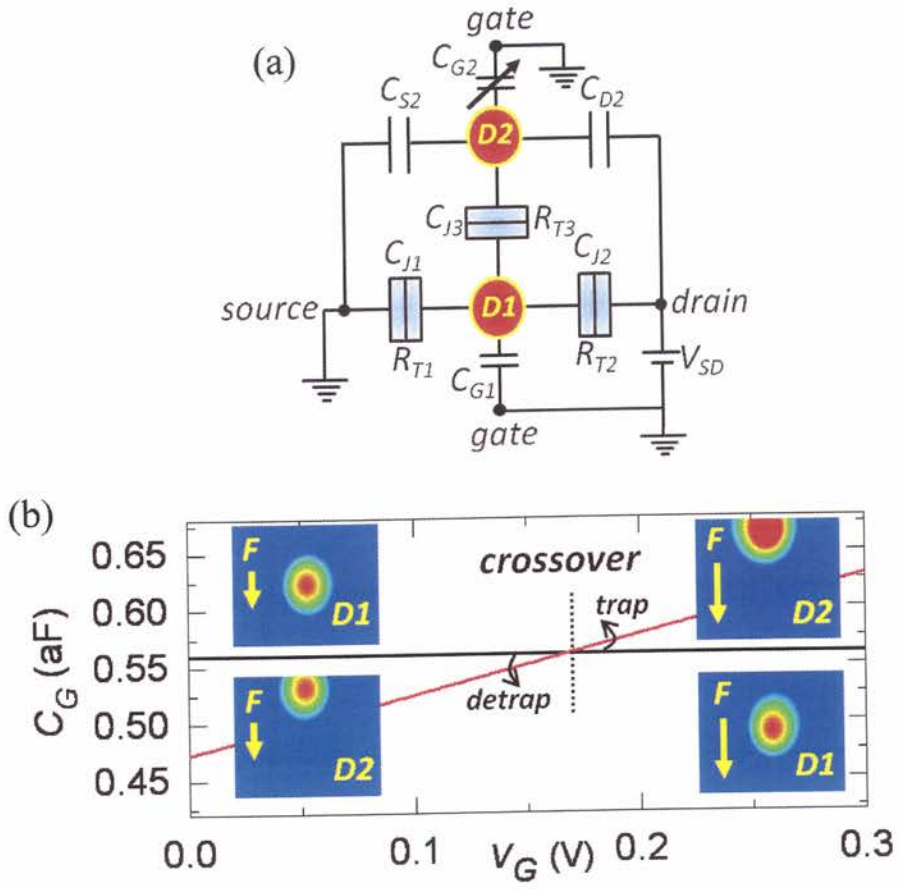


Fig.4. 11 (a) Equivalent circuit of two parallel coupled donor-QDs with variable gate capacitance. **(b)** $C_G - V_G$ dependence reflecting the donor-interface coupling under increasing electric field for the two donors: deeper donor *D1* (horizontal line) and superficial donor *D2* (inclined line).

In order to reproduce single-electron transfer characteristics in simulation, we model the two-donor system as two parallel QDs, as shown in the equivalent circuit of Figure 4.11 (a). Single-electron transport simulations are performed for this circuit within the orthodox Coulomb blockade theory. The two donors are physically separated by a tunnel barrier and, therefore, a tunnel junction is inserted

between them. Donor D_1, located close to the center of the channel in horizontal and vertical directions [68] works as the steppingstone in the conduction path and is coupled to source and drain by tunnel junctions ($C_{J1}R_{T1}$ and $C_{J2}R_{T2}$). Donor D_2 is expected to be displaced from the center towards the edge of the channel, where the potential barriers in the source-drain direction are higher for small voltages. Therefore, this donor is coupled to source and drain via non-tunnel capacitors (C_{S2} and C_{D2}). Other donors are also present in the device channel, but their energies are higher than the Fermi energy. In consequence, their effect can be basically incorporated in these tunnel barriers. The two donor-QDs are commonly coupled to the same gate.

Our purpose is to reproduce the hysteresis in the $I_{SD} - V_G$ characteristics by using the circuit shown in Figure 4.11 (a). However, this hysteresis should only involve the two states of each donor, i.e., one electron is transferred from a neutral donor to an ionized donor. When the donors are considered as QDs with fixed gate capacitances, single-electron transfer cannot be achieved unless other assistant electrons are involved in the process as explain in our fixed two dot system. In previous reports of two-classical-dot circuits with constant gate capacitances [38], [82], hysteresis observed as a signature of single-electron memory operation involves more than one elementary charge, although not explicitly described. For a two-donor system, only one electron can be involved in the transfer process. This

can only be explained if the gate capacitances of the two donors cross over at a certain gate voltage. This crossover induces an energetic transfer of the electron location in the two-donor system and it can only be realized by considering voltage-dependent donor-gate capacitances, as we incorporate in our simulations.

Figure 4.11 (b) shows the gate capacitances for the two donors with fixed depths as a function of V_G. The gate capacitance C_{G1} of the deeper donor, *D1*, is practically constant, while the gate capacitance C_{G2} of the superficial donor, *D2*, changes with V_G. The slope of this change reflects the donor depth below interface. At small V_G, C_{G2} can be even smaller than C_{G1} due to the reduced area towards the gate. A crossover between the gate capacitances of the two donors occurs at a certain V_G. We suggest that this capacitive crossover is crucial in determining the energetic transfer of an electron between the two donors. For small V_G's, when $C_{G2} < C_{G1}$, it is energetically favorable for the electron to occupy donor *D1*. After the crossover point, when $C_{G2} > C_{G1}$, the system energetically favors the electron transfer to donor *D2*. This can explain the origin of the single-electron transfer.

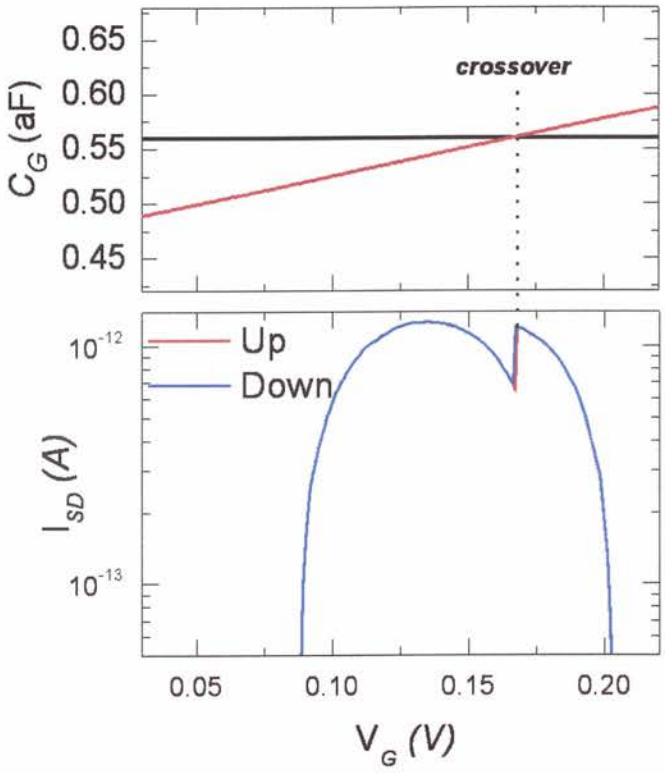


Fig.4. 12 Electron charging/discharging occurs on the crossover point, as marked by the dotted line.

However, the transfers just happen on the crossover point, as shown in Figure 4.12. In this case, we cannot observe the hysteresis anymore. We observed, however, that single-electron transfer occurs with a delay relative to the crossover voltage, which gives rise to a hysteresis between single-electron trapping and detrapping events. We monitored the dependence of the width of this hysteresis, ΔV_G, as a function of two factors: the trap donor's $C_G - V_G$ slope and the inter-donor resistance, $R_{D1D2,}$ which I will explain in the next section. When we introduce inter-tunnel resistance, we obtain the fine hysteresis shown in Figure 4.13 (a).

However, when we introduce a high inter-tunnel resistance and consider the trap donor location relatively far away from the interface, we observed complete shift hysteresis, as shown in Figure 4.13 (b).

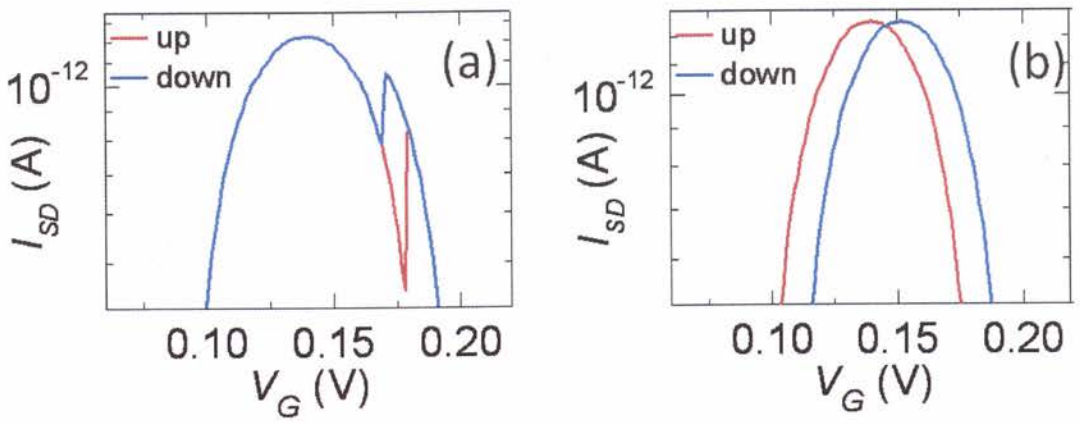


Fig.4. 13 (a) Electron charging/discharging occurs on the peak **(b)** Electron charging and discharging occur off the peak.

This hysteresis is dependent on the measurement time. If the measurement time is long, we cannot observe hysteresis as a signature of kinetic-delay effect. To prove that, we simulated characteristics as a function of measurement time, as shown in Figures 4.14 (a), (b), and (c). Figure 4.14 (a) shows the hysteresis for short-time measurement. When we increase the measurement time (medium), the hysteresis becomes smaller. When the measurement time is long, we could not see any hysteresis. This is due to the fact that the transition period for electrons to transfer is long, and as a result hysteresis does not appear because the electron transfer event happen close to the crossover voltage.

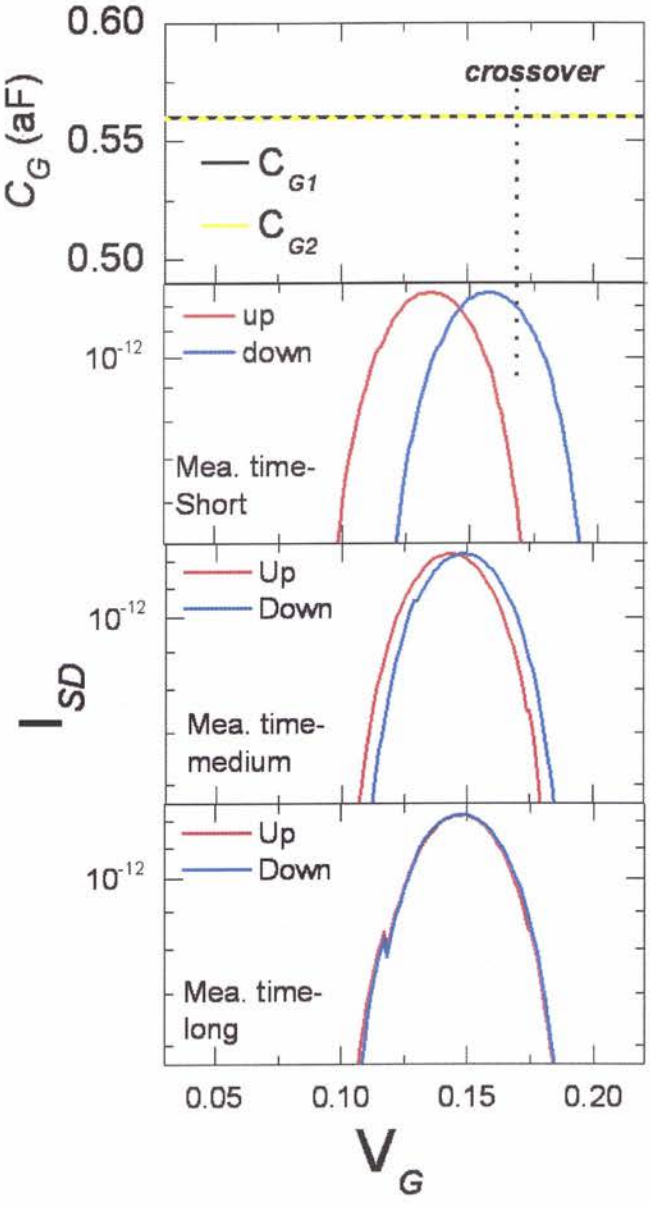


Fig.4. 14 **(a)** I-V characteristics for short measurement time **(b)** I-V measurement for medium measurement time **(c)** I-V measurement for long measurement time.

4.4.5 Donor-interface and donor-donor coupling effect on electron transfer

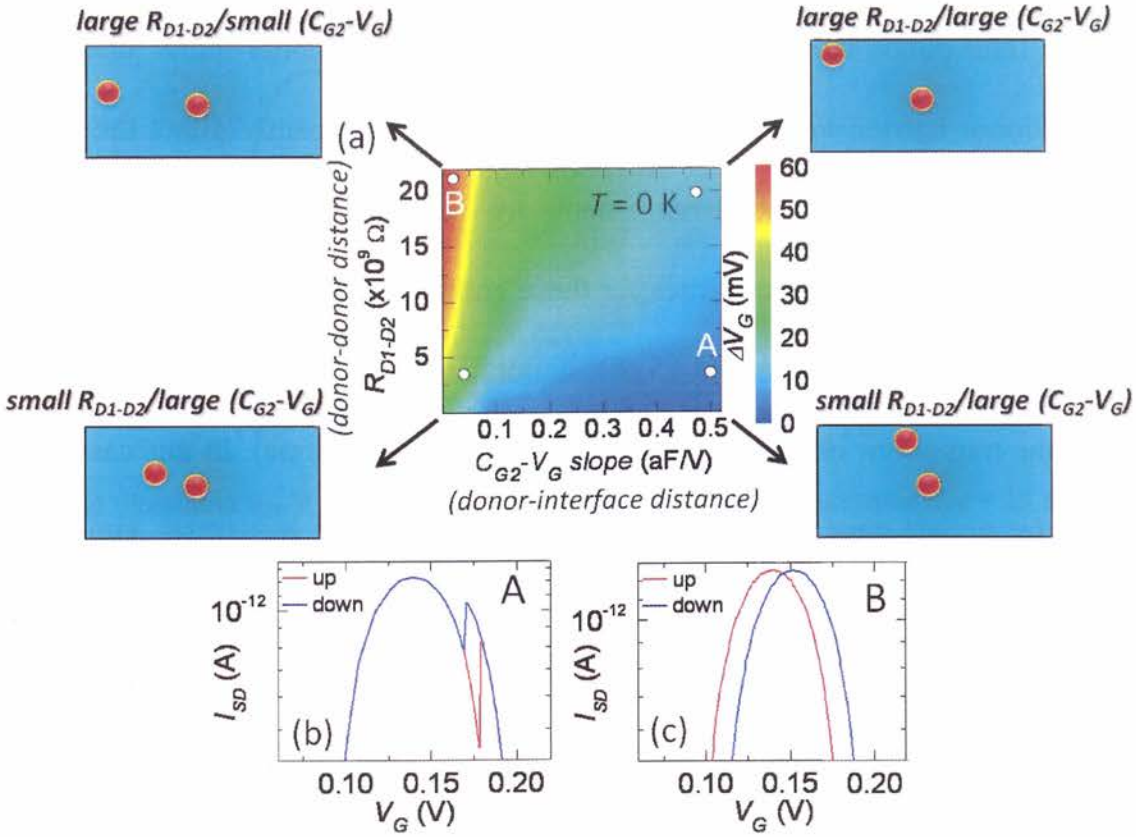


Fig.4. 15 (a) Contour plot of the voltage shift ΔV_G (difference between the voltages at which trapping and detrapping occur) as a function of $C_{G2} - V_G$ slope and donor-donor tunnel resistance. The schematic views at the four corners indicate donor position for the four white circle points. **(b)-(c)** Simulated $I_{SD} - V_G$ characteristics (upward and downward V_G ramping) for two cases, indicated in **(a)**: point A [**(b)**] and point B [**(c)**].

We observed, however, that single-electron transfer occurs with a delay relative to the crossover voltage, which gives rise to a hysteresis between single-electron trapping and detrapping events. We monitored the dependence of the width of this

hysteresis, ΔVG, as a function of two factors, as shown in Figure 4.15 (a).The slope can be correlated with donor-interface distance, as explained above in Figure 4.15. Inter-donor resistance can be correlated to the donor-donor distance, i.e., inter-donor barrier width. Both these parameters significantly affect the hysteresis width. Two opposite donor arrangements are indicated by point A and point B. The simulated $I_{SD} - V_G$ characteristics for these configurations are shown in Figure 4.15 (b) and 4.15 (c). For Figure 4.15 (b), donors are close to each other (small $R_{D1\text{-}D2}$) and the trap donor is close to interface (large $C_{G2} - V_G$ slope). In this case, electron transfer occurs near the crossover V_G, producing a fine hysteresis, similar to the experimental observation in Figure 3.10 (a). For Figure 4.15 (c), which corresponds to donors far from each other (large $R_{D1\text{-}D2}$) and the trap donor relatively far from interface (small $C_{G2} - V_G$ slope), electron transfer is significantly delayed relative to the crossover V_G. Thus, the current peak is totally shifted, similarly to the results shown in Figure. 3.11. The experimental results can, thus, be ascribed to these two different donor arrangements. From preliminary simulations, we also found that inter-donor capacitance can assist in further separating the current peaks. I used inter-donor capacitance C_{J3}= 10 aF and obtained completely separated peaks, as shown in Figure 4.16, which can be useful for applications. However, we also found complete peak separation in our experimental observation. More study is necessary to understand the inter-donor capacitance effect. Some studies are

already under way.

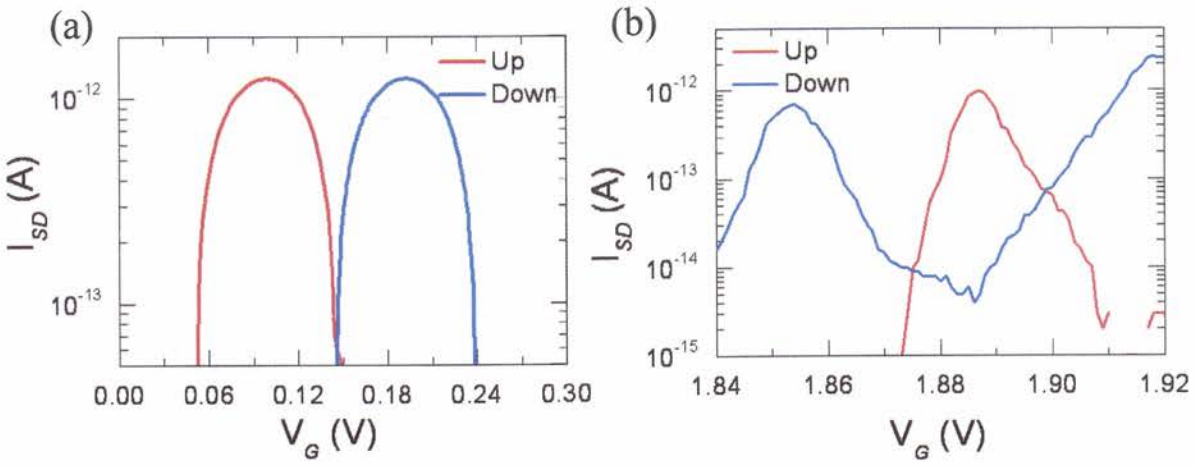


Fig.4. 16 (a) Simulated I_{SD}-V_G characteristics for high inter-tunnel capacitance C_{J3} = 10 aF **(b)** Experimental observation of I_{SD}-V_G characteristics shows complete peak separation.

4.4.6 Comparison between experimental and simulation results

From experimental results, we can observe the single-electron tunneling via one donor as the first peak of the $I_{SD} - V_G$ characteristics. By continuously increasing V_G, an electron can be shuttled to the trap donor and this change of the charge state will affect, at its turn, the single-electron conduction current. Similarly, if V_G is successively decreased, the electron should be eventually released from the trap. From the simulation results, we can see that for two-donor systems with variable donor-gate capacitance, simulation can successfuly reproduce the experimental results. In my simulation, the gate capacitance C_{G1} of the deeper donor, *D1*, is practically constant, while the gate capacitance C_{G2} of the superficial donor, *D2*,

changes with V_G. This gradual change of donor-gate capacitance C_{G2} causes a single-electron transfer from donor *D1* to donor *D2*. The experimental and simulation results are shown for comparison in Figure 4.17.

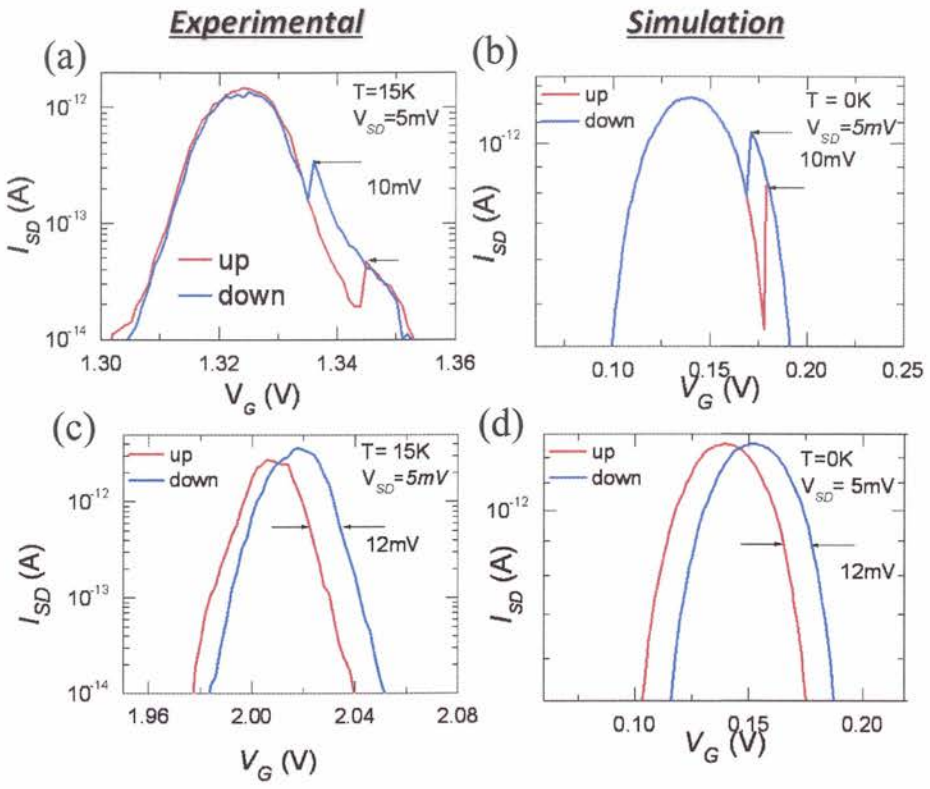


Fig.4. 17 Comparison between the experimental (a) and simulation (b) results, i.e., I_{SD}-V_G characteristics of charging effect on the peak. Comparison between the experimental (c) and simulation (d) result, i.e., I_{SD}-V_G characteristic of charging effect off the peak.

Conclusion

In this work, we demonstrated single-electron transfer between two donors in thin SOI-FETs. This is evidenced by the hysteresis on the first observable current peak in the current-voltage characteristics. The findings are supported by

simulation results for two parallel donor-QDs with limited occupancy. We show that single-electron transfer between two donors is only possible if the gate capacitances of the two donors cross over. By considering the behavior of donors near interfaces, we introduce a concept of voltage-dependent donor-gate capacitance to limit the number of electrons in each donor to one, thus successfully explaining single-electron transfer between two donors.

We also showed that the hysteresis is affected by the donor depth and donor-donor distance. These results can be useful in designing novel applications utilizing donor-donor interaction.

Chapter 5
Single-electron charging in triple-donor system

We already found that parallel double-donor system can produce hysteresis. This hysteresis is due to energetic and kinetic effects. However, for memory operation kinetic effect is a weak point from the viewpoint of long retention time. That is why energetically stable electron trap is necessary.

For that purpose, I investigated single-electron charging behavior in triple-donor system. Several other groups have recently reported preliminary measurements on triple quantum dot device [83], [84], [85], [86], [87]. I consider symmetric and asymmetric parallel-coupled triple-QD systems in my model. Figure 5.1 the case of the shows symmetric triple-donor system.

5.1 Symmetric triple-donor system

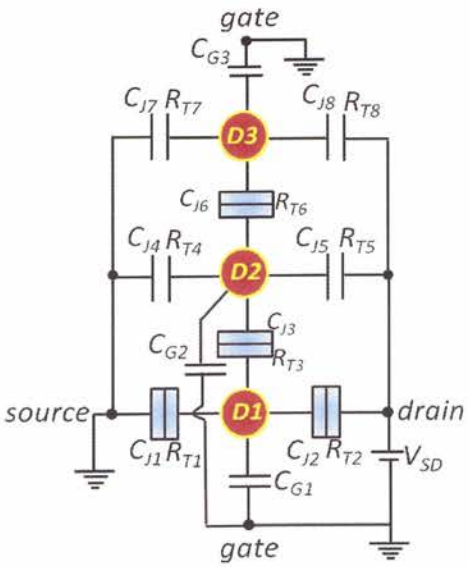
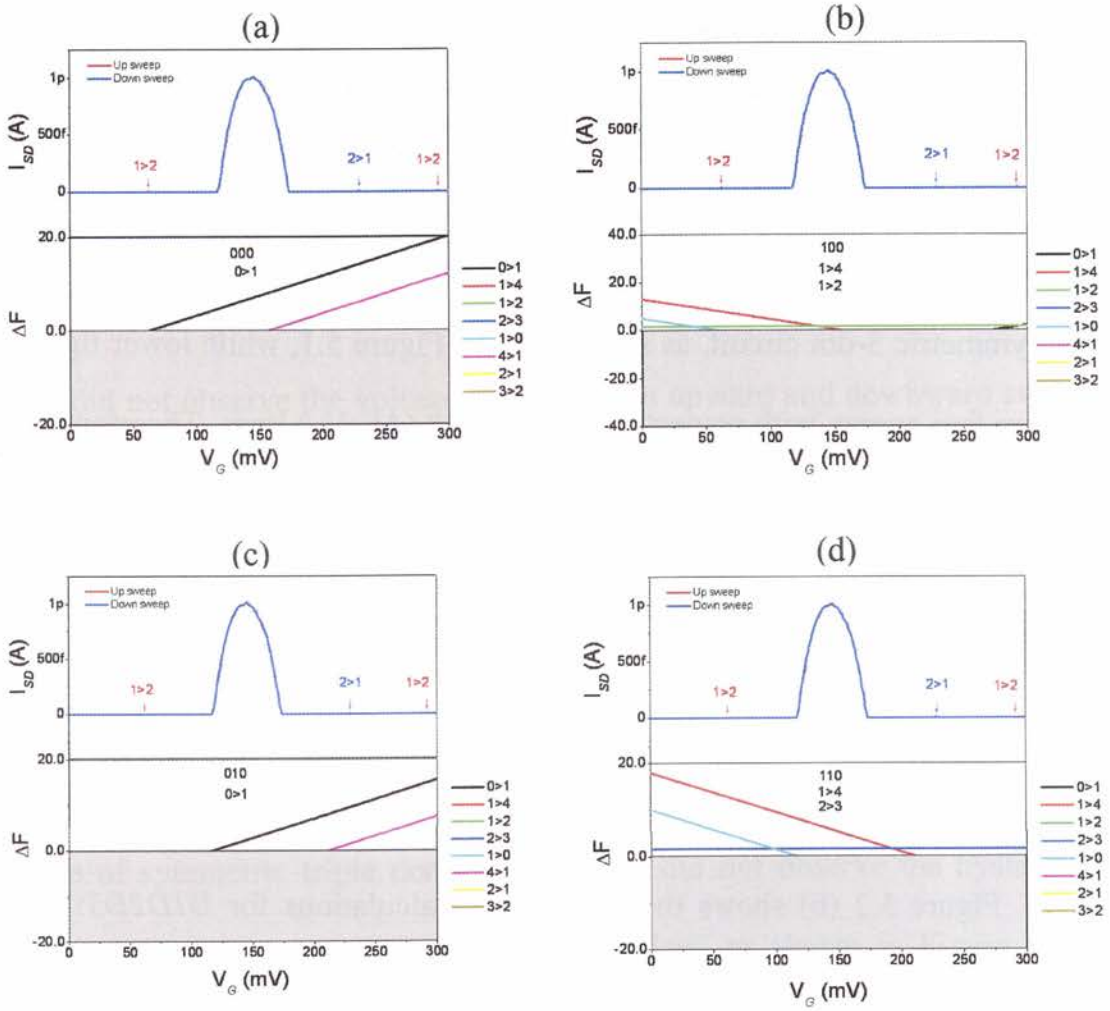


Fig.5. 1 Equivalent circuit for parallel triple-donor system.

At first, I consider the symmetric system for simulation. I used equal gate capacitances, C_{G1}, C_{G2} and C_{G3} are each 0.56 aF; tunneling capacitances C_{J1}, C_{J2}, C_{J3}, C_{J4}, C_{J5}, C_{J6}, C_{J7}, C_{J8} = 5 aF; tunneling resistances R_{T1}, R_{T2}, R_{T3}, $R_{T6} = 1 \times 10^9$ Ω and R_{T5}, R_{T6}, R_{T7}, $R_{T8} = 1 \times 10^{14}$ Ω, practically disconnecting the upper two dots from source and drain. So, electron is not allowed to enter from source or drain to dot 2 and dot 3. To understand details about electron movement in this 3 dot system, we calculated system free energy as shown Figure 5.2.



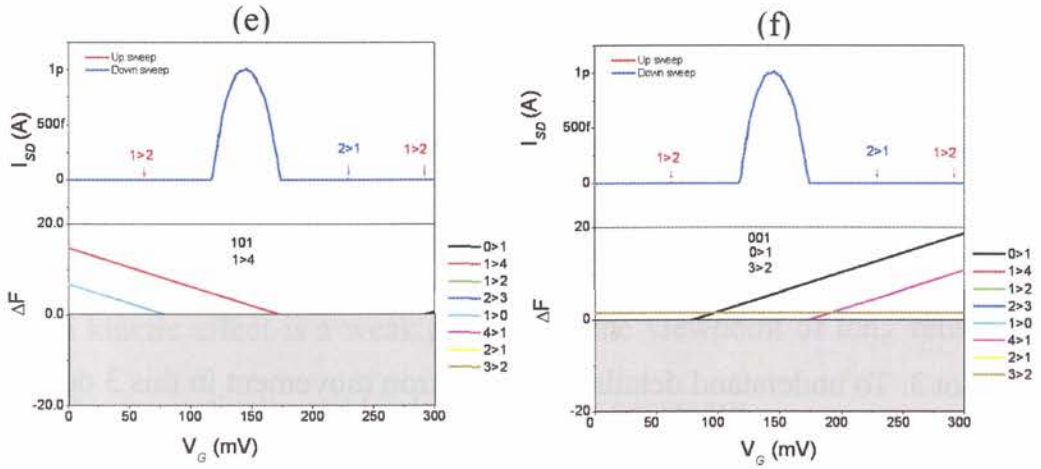


FIg.5. 2 (a-f) Electron transfer mechanism for symmetric triple-dot systems. Upper figures show I_{SD}-V_G characteristics. Lower figures show the system free energy calculations corresponding to the upper I_{SD}-V_G characteristics.

For all the Figures 5.2 (a-f), upper ones show simulated I_{SD}-V_G characteristics for symmetric 3-dot circuit, as shown also in Figure 5.1, while lower figures show system free energy with respect to gate voltage (ΔF-V_G) lines. Therefore, based on free energy calculations, we can understand the electron movement as follows.

Figure 5.2 (a) shows the free energy calculations for *D1D2D3*:000 charge state. At this stage, the favorable event is 0 > 1, as shown by the black inclined line, which means that one electron comes from source to dot 1. Now the charge state becomes *D1D2D3*:100.

Figure 5.2 (b) shows the free energy calculations for *D1D2D3*:100 charge state. At this stage, the favorable event is 1 > 2, as shown by the light green

horizontal line, which means that one electron comes from dot 1 to dot 2. Now, the charge state becomes *D1D2D3*:010.

Figure 5.2 (c) shows the free energy calculations for *D1D2D3*:010 charge state. Now, the favorable event is 0 > 1, which means that one electron will move from source to dot 1. Now, the charge state becomes *D1D2D3*:110.

Figure 5.2 (d) shows the free energy calculations for *D1D2D3*:110 charge state. Now, the event 2 > 3 is favorable for all the range of V_G, as shown by the blue horizontal line. One electron will move from dot 2 to dot 3. Now, the charge state becomes *D1D2D3*:101.

Figure 5.2 (e) shows the free energy calculations for *D1D2D3*:101 charge state. At this stage, event 1 > 4 is favorable. One electron will move from dot 1 to drain. Now, the charge state becomes *D1D2D3*:001.

We did not observe the voltage shift between upward and downward sweep. The reason why we did not observe the voltage shift may attributed to the fact that trapping and detrapping occur both at the same gate voltage. It means that the trapped electron immediately escapes from the trap donor.

5.2 Asymmetric triple-donor system

In case of symmetric triple donor system, we did not observe the hysteresis. Then, we considered asymmetric triple-donor system, as shown in Figure 5.3. I

purposely avoid showing the arm tunnel junction for donor *D2* and *D3*, as those are disconnected from source and drain, as mentioned earlier.

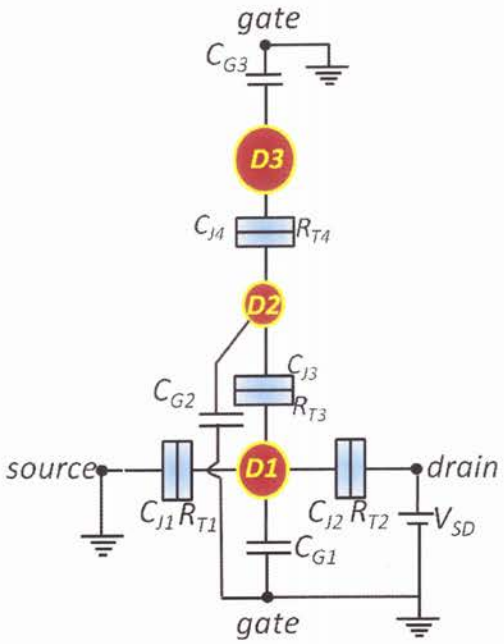
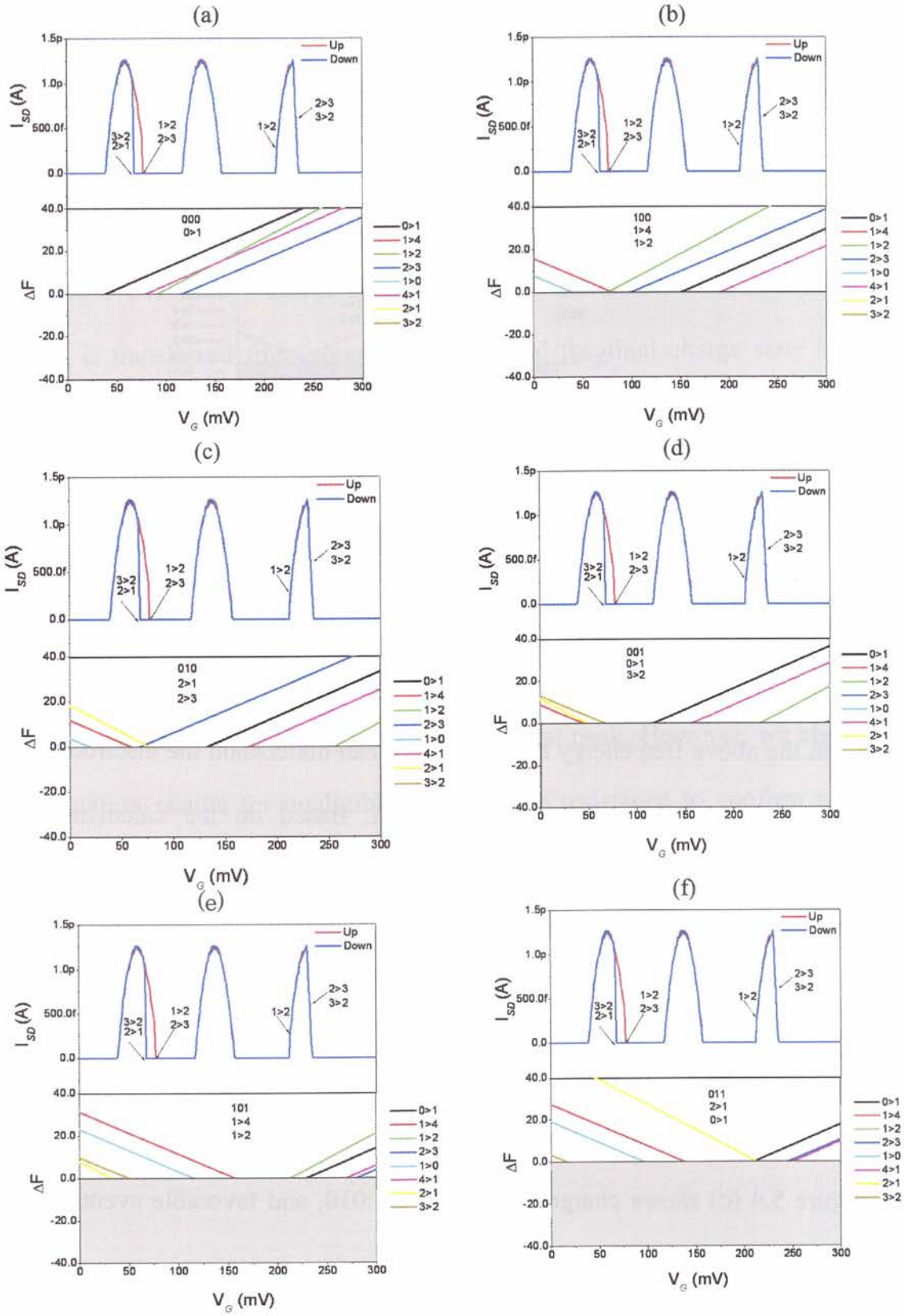


Fig.5. 3 Equivalent circuit of asymmetric triple-donor system.

To observe the hysteresis caused by multiple tunneling in three-dot system, I considered the asymmetric system for simulation. I used gate capacitances C_{G1} = 0.56 aF, C_{G2} = 0.2 aF and C_{G3} = 1 aF; tunneling capacitances C_{J1}, C_{J2}, C_{J3}, C_{J4}, = 5 aF; tunneling resistances R_{T1}, R_{T2}, R_{T3}, R_{T4} = 1×10^9 Ω. To understand details about electron movement in this asymmetric 3-dot system, we calculated system free energy, as shown Figure 5.4.


(a)
(b)
(c)
(d)
(e)
(f)
Up
Down
I_{SD} (A)
V_G (mV)
ΔF
000
0>1
100
1>4
1>2
010
2>1
2>3
001
3>2
101
011
0>1
1>4
1>2
2>3
1>0
4>1
2>1
3>2

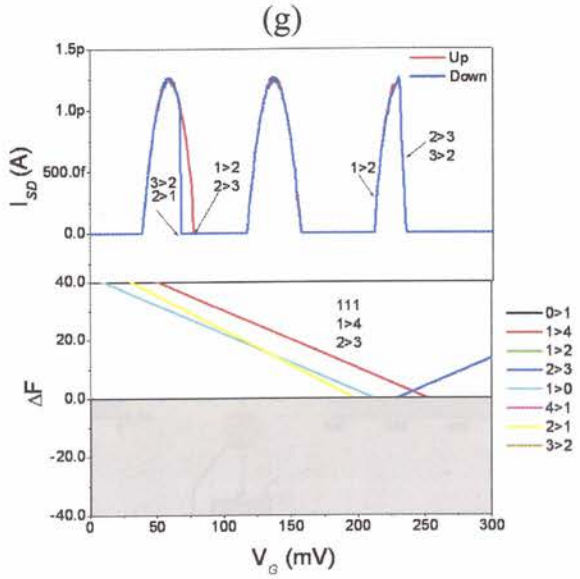


FIg.5. 4 (a-g) Electron transfer mechanism for asymmetric triple-dot systems. Upper figure show I_{SD}-V_G characteristics. We observe hysteresis on the first peak between upward and downward sweep. Lower figures show the system free energy calculations corresponding to the upper I_{SD}-V_G characteristics.

From the above free energy calculation we can understand the electron transfer mechanism for asymmetric triple-dot system. Based on the calculations, the electron transfer occurs in the following way.

Figure 5.4 (a) shows charge state *D1D2D3*:000, and favorable event is 0 > 1. Electron is transferred from source to dot 1.

Figure 5.4 (b) shows charge state *D1D2D3*:100, and favorable event is 1 > 2. Electron is transferred from dot 1 to dot 2.

Figure 5.4 (c) shows charge state *D1D2D3*:010, and favorable event is 2 > 3. Electron is transferred from dot 2 to dot 3.

Figure 5.4 (d) shows charge state *D1D2D3*:001, and favorable event is 0 > 1. Electron is transferred from source to dot 1.

Figure 5.4 (e) shows charge state *D1D2D3*:101, and favorable event is 1 > 2. Electron is transferred from dot 1 to dot 2.

Figure 5.4 (f) shows charge state *D1D2D3*:011, and favorable event is 0 > 1. Electron is transferred from source to dot 1, and the final charge state becomes *D1D2D3*:111.

In case of asymmetric 3-dot systems, we observe hysteresis appearing on the first peak. This hysteresis is due to events 0 > 1 and 1 > 2, both happening at the same gate voltage V_G = 77 mV, i.e., one electron becomes trapped in dot 3. In the same way, detrapping happens by events 3 > 2 and 2 > 1 at V_G = 67 mV. This multiple tunneling causes the hysteresis on the first peak. However, we also check the simulation results for negligible intermediate resistance to confirm energetic hysteresis effect; we found that even for small intermediate resistances, i.e., R_{T2}, R_{T3} = $1\times10^{6}\Omega$, hysteresis still appeared on the peak, which means that this hysteresis is due to the energy of the system and not to a kinetic delay, which is a promising feature for memory application. More work is required to fully clarify this point and some analysis is under way.

Chapter 6
Conclusion and suggestions

The experimental results presented in our manuscript, we believe, strongly suggest that the single-electron trapping in the second donor occurs from the first donor working as a steppingstone for conduction.

In this study, we focus only on the first conduction peak. This peak is ascribed to single-electron tunneling via a single donor, having the lowest electronic potential in the channel. In the data shown in Figure 3.9 (a), it can also be seen that the second conduction peak is well separated in voltage (i.e., energy) from the first peak. On this first peak, we observe an abrupt current jump, which indicates trapping in another donor. The electron trapping in the second donor, presented in this manuscript, happens only on the first current peak. It is thus naturally considered that this trapping has a deterministic correlation with the first-donor electron. This means that trapping does not occur if current does not flow through the conduction donor, which strongly suggests that trapping is due to transfer from the conduction path. However, we cannot eliminate the possibility of electron trapping via different paths, since the above consideration is not perfectly evidenced.

The time-resolved measurements exhibit a two-level signal, suggesting a two-level trap. This is in agreement with the characteristics of a donor (ionized or

neutralized). Therefore, the trap is also *one donor*. Thus, one electron is switched between two donors: the donor acting as steppingstone for conduction and the trap donor.

Our simulations support the experimental findings. In simulations, we incorporated voltage-dependent donor-gate capacitances to realistically describe the donor-induced quantum dots.

Single-electron switching between two donors means that one electron moves from a neutral donor (containing one electron) to an ionized donor (lacking one electron), and that this transfer is reversible. The two-donor system has a limited number of occupancies since each donor can only contain 0 or 1 electron. We described this two-donor system by a two-dot circuit that contains the voltage-dependent donor-gate capacitances. The reasons for this approach are given below.

In a two-dot circuit with fixed gate capacitances, it is theoretically clear that single-electron switching cannot be realized without the assistance of at least one more electron. For an intuitive explanation, let's assume that the gate capacitance of dot 1 (C_{G1}) is larger than the gate capacitance of dot 2 (C_{G2}). In this situation, the <10> charge configuration, i.e., one electron in dot 1 and no electron in dot 2, is energetically favored, while the <01> configuration cannot be achieved. When a second electron is added to dot 1, i.e., <20> configuration, this electron can be transferred into dot 2, leading to a charge configuration of <11>. This mechanism I

already explained in section 4.2.2, which indicates the fact that assistant electrons are involved in the single-electron energetic switching between two dots with fixed gate capacitances. This cannot be the case of donor-induced dots, for which the electron occupancy must be limited to one under normal temperature conditions.

Previous studies also indicated that single-electron memory operation is feasible: K. Yano *et al.* (IEEE Trans. Electron Devices, 41, 1628, 1994) and A. Fujiwara *et al.* (Appl. Phys. Lett., 67, 2957, 1995). In these papers, a fixed-parameter circuit was assumed to explain the single-electron trapping in one dot as hysteresis in the current-voltage characteristics. However, although the number of electron occupancy is not explicitly discussed in these papers, it is most probable that it is similar to the model described above. More than one electron should be involved in the trapping and detrapping of one electron in a memory dot.

In conclusion, due to the limited occupancy of a donor-induced dot, it is not possible to explain donor-donor one-electron switching when the donors have fixed gate capacitances. The only way is to consider variable donor-gate capacitances that allow a crossover of the C_G's of the two donors. This crossover corresponds to an energy-driven one-electron switching between the two donors.

We also point out that the variable donor-gate capacitance model is also justified in terms of device structure. In our devices, donors are very near interfaces and the donor-dot expands at the interface with increasing electric field. This point

is clearly described in this thesis.

To establish the grounds of single-donor memory concept, additional studies are under way. For example, we found in case of variable donor-gate capacitance that two-donor system can produce the hysteresis, but we need to incorporate high tunnel resistance. This means that, for a two-donor system, electron transfer occurred energetically, but to introduce hysteresis we need to consider high tunnel resistance, which is not effective for memory operation since the retention time is expected to be significantly low.

Energetic electron-trapping is necessary to generate long retention time for memory operation. That is why at present we focus on the three-dot system. Some preliminary results that we have observed give us a hope that three-dopant systems will be a good candidate for future memory technology. More work is under way.

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List of Publications

1. **E. Hamid,** D. Moraru, J. C. Tarido, S. Miki, T. Mizuno, M. Tabe, "***Single-electron transfer between two donors in nanoscale thin silicon-on-insulator field-effect transistors***", Applied Physics Letters, Vol. 97, no. 26, pp. 262101 (2010).

2. **E. Hamid,** J. C. Tarido, S. Miki, T. Mizuno, D. Moraru, and M. Tabe, "***Charging phenomena of a single electron in P-doped Si SOI MOSFETs***", *IEICE Technical Report*, Vol. 110, no. 31, pp. 23-26 (2010).

3. M. Tabe, D. Moraru, **E. Hamid,** M. Anwar, A. Udhiarto, R. Nakamura, S. Miki, and T. Mizuno, "***Si single-dopant devices and their characterization***", *IEICE Technical Report*, Vol. 110, No. 109, pp. 131-136 (2010).

4. D. Moraru, **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, and M. Tabe, "***Memory effects based on dopant atoms in nano-FETs***", Advanced Materials Research (to be published).

List of Conferences

International

1. M. Tabe, D. Moraru, **E. Hamid**, J. C. Tarido, M. Anwar, R. Nowak, Y. Kawai, R. Jablonski, and T. Mizuno – ***Atom devices based on single-dopants in silicon nanostructures*** (oral – invited), Villa Conference on Interactions Among Nanostructures (VCIAN) –(Las Vegas, USA), **Apr. 2011.**

2. M. Tabe, D. Moraru, **E. Hamid**, M. Anwar, A. Udhiarto, R. Nowak, S. Miki, R. Nakamura, Y. Kawai, J. C. Tarido, and T. Mizuno – ***Si single dopant devices*** (oral – invited), International Symposium on Nanoscale Transport and Technology (ISNTT 2011) –(Atsugi, NTT BRL), **Jan. 2011**.

3. D. Moraru, J. C. Tarido, R. Nakamura, **E. Hamid**, T. Mizuno, and M. Tabe – ***Single-electron transport via single and multiple donors in nanoscale Si-FETs*** (oral), Hamamatsu, **Nov. 2010**.

4. D. Moraru, **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, and M. Tabe – ***Memory effects based on dopant atoms in nano-FETs*** (oral), (Riga, Latvia), Proceedings, pp. 86-87, **Aug. 2010**.

5. M. Tabe, D. Moraru, **E. Hamid**, M. Anwar, A. Udhiarto, R. Nakamura, S. Miki, and T. Mizuno – ***Si single-dopant devices and their characterization*** (oral – invited), (Tokyo), Proceedings / IEICE Technical Report, Vol. 110, No. 109, pp. 131-136, **Jun. 2010.**

6. **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, D. Moraru, and M. Tabe – ***Single-dopant memory effect in P-doped Si SOI-MOSFETs*** (oral), Silicon Nanoelectronics Workshop, (Honolulu, Hawaii), Workshop Abstracts, pp. 45-46, **Jun. 2010**.

National

1. J. C. Tarido, **E. Hamid**, D. Moraru, R. Nakamura, S. Miki, T. Mizuno, and M. Tabe – ***Possibility of electron transfer between two donors via interface in doped nanoscale Si FETs,*** 58th Spring National Conference (応用物理学会-春)-(Atsugi, Kanagawa), **Mar. 2011.**

2. **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, D. Moraru, and M. Tabe – ***Single-electron memory effect in double-donor and triple-donor systems,*** 58th Spring National Conference (応用物理学会-春) –(Atsugi, Kanagawa), **Mar. 2011.**

3. D. Moraru, **E. Hamid**, J. C. Tarido, S. Miki, R. Nakamura, T. Mizuno, and M. Tabe – ***Single-electron transfer between two donors in thin nanoscale silicon transistors*** (oral), IEICE ED/SDM Meeting (Hokkaido Univ., Sapporo), **Feb. 2011**.

4. **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, D. Moraru, M. Tabe – ***Single-electron charging by extension of dopant-induced quantum dot at interfaces under electric field*** (oral), JSAP 71st Autumn National Conference, (Nagasaki), **Sept. 2010**.

5. **E. Hamid**, J. C. Tarido, S. Miki, D. Moraru, T. Mizuno, and M. Tabe – ***Charging phenomena of a single electron in P-doped SOI-MOSFETs*** (oral), ED/SDM Meeting, (Hamamatsu), Proceedings / IEICE Technical Report, Vol. 110, no. 31, pp. 23-26, **May 2010**.

6. **E. Hamid**, J. C. Tarido, S. Miki, T. Mizuno, D. Moraru, and M. Tabe – ***Simulation and experimental study of single electron trapping in doped nanoscale FETs*** (oral), 57th Spring National Conference, (Tohoku Univ.), **Apr. 2010**.

7. D. Moraru, **E. Hamid**, J. C. Tarido, A. Udhiarto, S. Miki, T. Mizuno, and M. Tabe – ***Characteristics of dopant SOI-MOSFETs and photon effects*** (poster), Silicon Nanotechnology Postscaling Meeting, (Tokyo), **Jan. 2010**.

8. J. C. Tarido, **E. Hamid**, S. Miki, D. Moraru, T. Mizuno, and M. Tabe – ***Single dopant memory effect in ultra-thin silicon field-effect transistors*** (oral), Surface Science Symposium, (Nagoya), **Dec. 2009**.

9. **E. Hamid**, J. C. Tarido, S. Miki, M. Anwar, M. Ligowski, T. Mizuno, D. Moraru, and M. Tabe – ***Possibility of single electron trapping by a single dopant in doped nanoscale FETs*** (oral), JSAP 70th Autumn National Conference, (Toyama), **Sept. 2009**.