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Effects of substrate voltage on noise characteristics and hole lifetime in SOI metal-oxide-semiconductor field-effect transistor photon detector

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Abstract: Low-frequency noise and hole lifetime in silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) are analyzed, considering their use in photon detection based on single-hole counting. The noise becomes minimum at around the transition point between front- and back-channel operations when the substrate voltage is varied, and increases largely on both negative and positive sides of the substrate voltage showing peculiar Lorentzian (generation-recombination) noise spectra. Hole lifetime is evaluated by the analysis of drain current histogram at different substrate voltages. It is found that the peaks in the histogram corresponding to the larger number of stored holes become higher as the substrate bias becomes larger. This can be attributed to the prolonged lifetime caused by the higher electric field inside the body of SOI MOSFET. It can be concluded that, once the inversion channel is induced for detection of the photo-generated holes, the small absolute substrate bias is favorable for short lifetime and low noise, leading to high-speed operation.

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1. Introduction

A type of single-photon detector, which directly counts photo-generated and stored (or trapped) single charges by a sensitive electrometer, is drawing attention because of its potential as a photon-number-resolving detector [1–8]. Quantum dot field-effect transistor (QDFET) [2–4] utilizes the GaAs/AlGaAs two-dimensional electron gas (2DEG) channel as an electrometer to detect the photo-generated and trapped holes in the InAs self-organized QDs. Single-electron photodetector (photo-SET) [5,6] with nanocrystal silicon (nc-Si) dots formed by the deposition and annealing of Si-rich oxide utilizes single-electron transistor (SET) as an electrometer to detect photo-generated single charges trapped in the dot or Si/oxide interface. We have also studied the scaled-down silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor (MOSFET) [7,8], in which photo-generated holes are stored below the negatively biased gate, and are detected as changes in the bottom-channel electron current. This SOI MOSFET is practically very attractive in that it can be manufactured by the standard Si integrated circuit technology and features small dark counts of ~10^{-2} s^{-1} at room temperature, but issues remain such as low quantum efficiency (QE) and the slow operation speed [7], and this report intends to address the latter.

There are two main factors affecting the operation speed. One is the drain current noise. If the noise spectral density, the required signal-to-noise ratio for discriminating the current levels, and the charge sensitivity (change in the drain current) to a single hole are S_{Id} [A^2/Hz], SNR, and ΔI_d [A/hole], respectively, the maximum count rate can be roughly estimated as $(\Delta I_d/SNR)^2/S_{Id}$ [s^{-1}] indicating the low noise is required for high-speed operation. The other factor is the hole lifetime in the body of SOI MOSFET. In order to avoid the saturation of the number of stored holes at a high photon incident rate, short lifetime is desirable as long as the short output pulses can be resolved. In this report, we will describe the behavior of the drain current noise and the hole lifetime under different substrate voltages in search of optimum operation condition of the SOI MOSFET as a photon detector.

2. Experimental

Although the original SOI MOSFET photon detector [7] had a special double-gate structure with a short lower gate (LG) and a long upper gate (UG) covering the p^--doped offset area between LG and n^+-doped source/drain, we select the ordinary n-channel fully-depleted (FD) SOI MOSFET without offset region [8] as shown in Fig. 1 considering its structural simplicity and versatility, and the device is fabricated in a 300-mm-wafer facility for Si integrated circuits to ensure the reproducibility.

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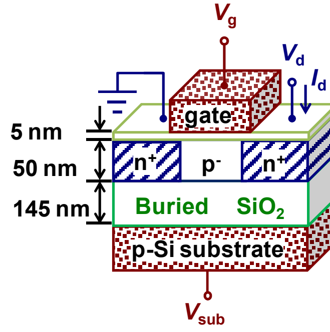

Fig. 1. Schematic diagram of the SOI MOSFET. Thicknesses of buried oxide, SOI and gate oxide are 145, 50 and 5 nm, respectively.

It has n^+ poly-Si-gate and p^- channel region with dopant concentration less than 10^{15} cm^{-3}. The SOI is of a wafer-bonding type supplied by Soitec S.A [9]. Thicknesses of buried oxide, SOI and gate oxide are 145, 50 and 5 nm, respectively. The gate length is fixed at 300 nm, and the channel width is varied among 90, 95 and 110 nm. In the noise measurement and the hole lifetime analysis, we changed the substrate voltage V_{sub}, while keeping the drain current at the constant level of 1 nA by adjusting the front gate voltage V_g. The drain current noise was measured in dark condition at 300 K, and the hole lifetime was evaluated by the analysis of drain current histograms for different levels of light intensity also at 300 K.

3. Results and discussion

3.1. Analysis of drain current noise

Figure 2 shows an example of I_d-V_g characteristics with V_{sub} as a parameter ranging from −10 to 10 V. Drain voltage V_d is kept at 50 mV. From these data, front-gate threshold voltage V_{th} corresponding to the I_d of 1 nA is extracted for setting the operation condition and further analysis. Figure 3 shows noise power for the bandwidth of 5 Hz, and the threshold voltage V_{th} plotted against the substrate voltage for various channel widths. In the V_{th}-V_{sub} characteristics, the deflection point 1 corresponds to the transition point between front- and back-channel operations, and the deflection point 2 to the transition between inversion and accumulation conditions at the buried oxide/substrate interface [10].

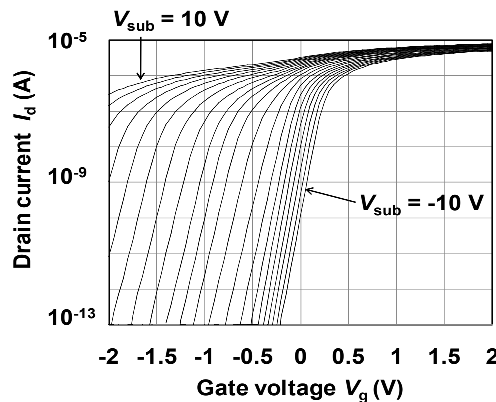

Fig. 2. I_d-V_g characteristics with V_{sub} as a parameter. Drain voltage V_d is kept at 50 mV. Device sizes are L = 300 nm and W = 110 nm.

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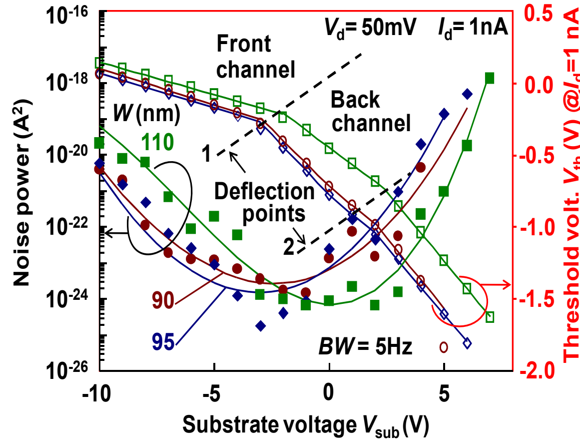

Fig. 3. Noise power and front-gate threshold voltage V_{th} at 1 nA as a function V_{sub}. The gate length is fixed at 300 nm, channel width is varied among 90, 95 and 110.

The noise levels show horseshoe shape, and become low at around the deflection point 1 and in the back-channel region between deflection points 1 and 2. This behavior is common for three different channel widths W, although a slight inverse narrow-channel effect [11], i.e. the reduction of V_{th} for smaller W, can be seen.

Figure 4(a) shows the drain current noise spectra for front-channel operation. The drain current was kept at 1nA (substreshold operation), while the substrate voltage was varied from −10 to −3V. At V_{sub} = −3V the usual $1/f$ noise spectrum is observed, which can be explained by the McWhorter's model [12] based on the charge fluctuation in the slow oxide traps near the Si/oxide interface caused by the carrier tunneling to and from the inversion channel, and moreover includes the contributions of both front and back interfaces (coupling effects) in the present case of FD SOI MOSFET [13].

As the V_{sub} decreased, an excess Lorentzian noise begin to evolve at V_{sub} = −5V which corresponds to a weakly accumulated back interface, when the magnitude of V_{sub} increases the noise spectra asymptotically approach a single $1/f^2$ line, indicating that the Lorentzian plateau level and time constant increase simultaneously. Figure 4(b) shows the noise spectra for back-channel operation in $-3 \le V_{sub} \le 4$V. The similar behavior of the evolution of the noise spectra can be observed, when the front interface is driven toward accumulation.

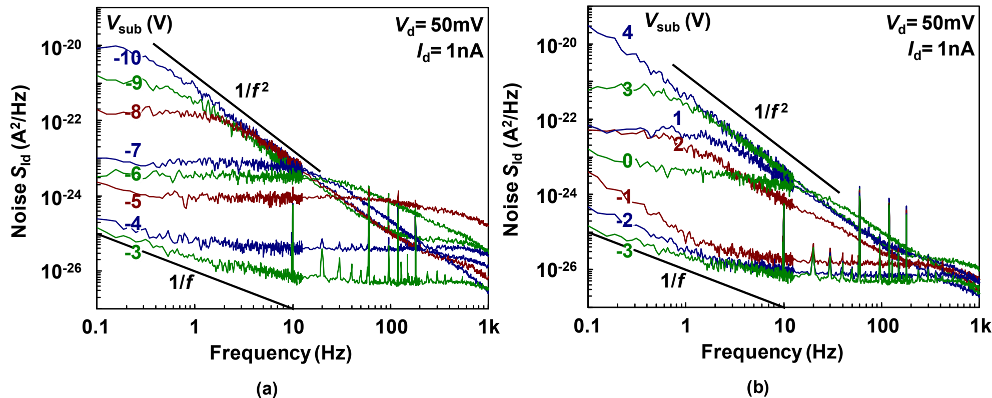

Fig. 4. Drain current noise spectra for (a) front-channel ($-10 \le V_{sub} \le -3$V), and (b) back-channel ($-3 \le V_{sub} \le 4$V) operations. Device sizes are L = 300 nm and W = 95 nm.

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In SOI MOSFET, the Lorentzian excess noises are often associated with the body potential fluctuation caused by several mechanisms of majority carrier generation [13–15], such as (a) impact ionization, (b) gate-induced drain leakage (GIDL) and other drain-body junction leakage, (c) tunneling through a thin gate oxide, (d) tunneling between back-gate-induced (BGI) accumulation layer and source/drain region, etc. However, these floating-body (FB) induced excess noises are not likely in the present device primary due to its FD operation, in which lower potential barrier at the source/body junction alleviates the accumulation of the majority carriers. In addition, low drain voltage of 50 mV, nearly symmetric behavior of the noise with respect to V_{sub}, and thick gate oxide of 5 nm are also incompatible with the mechanisms (a), (b), and (c), respectively. BGI Lorentzian noise (d) was actually reported in FD SOI MOSFET [16], but the Lorentzian time constant decreased as $|V_{\mathrm{sub}}|$ increased, which contradicts the behavior observed in the present experiment. Apart from the above FB mechanisms, D. S. Ang, et al. reported the very similar evolution of the noise spectra in the transition from FD to near FD operation, caused by the generation-recombination (GR) processes at bulk defects in the depleted SOI layer [17]. In our device, as can be seen in Fig. 4 (a) and 4(b), the asymptotic $1/f^2$ lines for both negative and positive V_{sub}, i.e. front- and back-channel operations, are quantitatively the same. This symmetric behavior strongly suggests the origin of the GR noise in the present device is not located at the front or back interface, but in the depleted SOI layer. This observation also excludes the possibility of random telegraph signal (RTS) [18], which is caused by the charge fluctuation in a single oxide trap and possibly shows the Lorentzian spectrum, because the individuality of the oxide traps in energy level and location in the oxide cannot lead to the common noise spectrum for both front- and back-channel operations.

3.2. Analysis of hole lifetime

Figure 5 shows typical drain current waveforms for different levels of light intensity at the wavelength of 550 nm. Baseline current is adjusted to 1 nA by V_{g}, and each waveform is shifted for clarity. V_{d} and V_{sub}, are 0.05 and 1.49 V, respectively. In this figure, we can see that the photo-generated holes modulate the drain current to discrete levels corresponding to the number of stored holes below the gate n_{h}, while the operating condition is set to $V_{\mathrm{g}} < 0$ and $V_{\mathrm{sub}} > 0$, so that the electrons flow in the back-channel. Note that, in dark condition, we could not observe signal exceeding the level of $n_{\mathrm{h}} = 1$, or RTS-like behavior. Actually, the randomness in the waveforms of Fig. 5 is caused by the statistical fluctuation of the photon arrival (hole generation) and hole recombination, which follow the Poisson process.

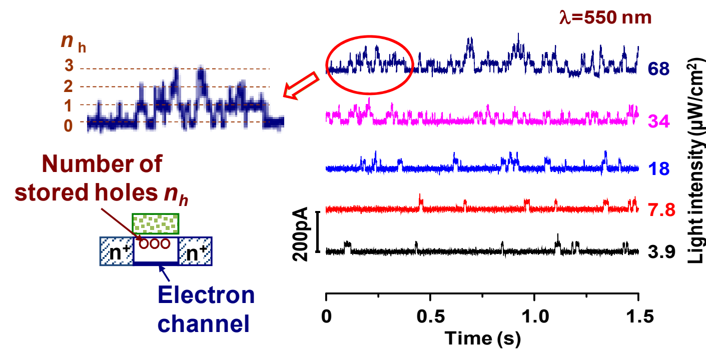

Fig. 5. Typical drain current waveforms at 300 K for different levels of light intensity at the wavelength of 550 nm. Baseline current is adjusted to 1 nA by V_{g}, and each waveform is shifted for clarity. The inset shows the enlarged waveform with discrete current levels corresponding to the number of holes n_{h} stored below the negatively biased gate. V_{d} and V_{sub} are 0.05 and 1.49 V, respectively. Device sizes are $L = 300$ nm and $W = 110$ nm.

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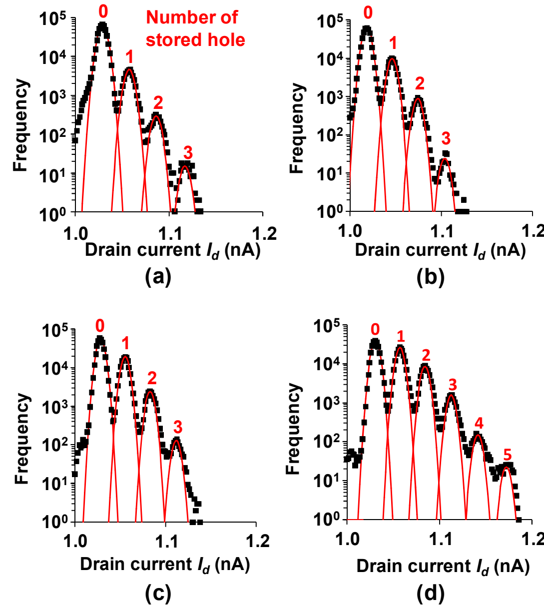

Fig. 6. Histograms of drain current for (a) V_{sub} = 1.27 V, (b) V_{sub} = 1.49 V, (c) V_{sub} = 1.72 V, and (d) V_{sub} = 1.93 V with different V_{sub} to keep the baseline drain current at the same level of 1 nA under the continuous light illumination of 34 μW/cm^2. The first, second, third, and fourth peaks correspond to the number stored holes of 0, 1, 2 and 3, respectively. Data acquisition time period and time step are 2.45 s and 49 μs, respectively, and 50000 (= 2.45 s / 49 μs) data points (current values) are classified into bins with a width of 2 pA. Device sizes are L = 300 nm and W = 110 nm.

As described in [7], the evolution of the state probability corresponding to each n_h can be explained well by the rate equation taking the hole generation and recombination rates into account, and this is the basis of the hole lifetime analysis.

Figure 6 shows the histograms of drain current for (a) V_{sub} = 1.27 V, (b) V_{sub} = 1.49 V, (c) V_{sub} = 1.72 V, and (d) V_{sub} = 1.93 V with different V_g to keep the baseline drain current at the same level of 1 nA. The closed symbols are obtained data and solid lines are fitting curves with Gaussian distribution. The peaks from left to right correspond to the number of stored holes of 0, 1, 2 and 3. It can be seen that the peaks in the histogram corresponding to the larger number of stored holes become higher as the V_{sub} increases. This may be caused by the longer hole lifetime, higher light absorption efficiency or higher collection efficiency of the photo-generated holes.

In order to understand the bias dependence of the light absorption and hole collection, hole generation rate is plotted against the light intensity in Fig. 7. There is proportionality between hole generation rate and incident light intensity regardless of V_{sub}, indicating that light absorption or hole collection efficiencies is not much changed by the bias condition. This also means that the hole lifetime can be controlled without affecting the nominal QE (as defined by the fraction of photons entering the detection area that are counted), which amounts to 0.15% in this case assuming the detection area of 300 × 110 nm^2.

The hole lifetimes are obtained as fitting parameters to describe the evolution of drain current histogram based on the rate equation under steady state conditions, $f_i / \tau_i = f_{i-1} R$ and $\Sigma f_i = 1$, where τ_i and f_i are hole lifetime and probability of state corresponding to hole number i, and R is hole generation rate [7]. The hole lifetimes at different V_{sub} are depicted in Fig. 8. It can be seen the hole lifetime increases significantly as V_{sub} increases. It is estimated that higher V_{sub} (higher transverse electric field) separates the stored hole and electron more effectively, and reduces the probability of recombination, leading to the longer lifetime.

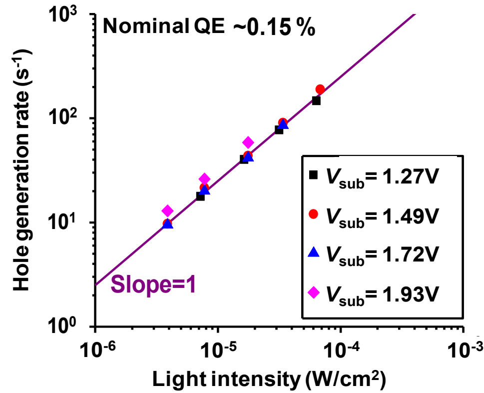

Fig. 7. Hole generation rate as a function of incident light intensity for each bias condition. Slope of the fitting line is one.

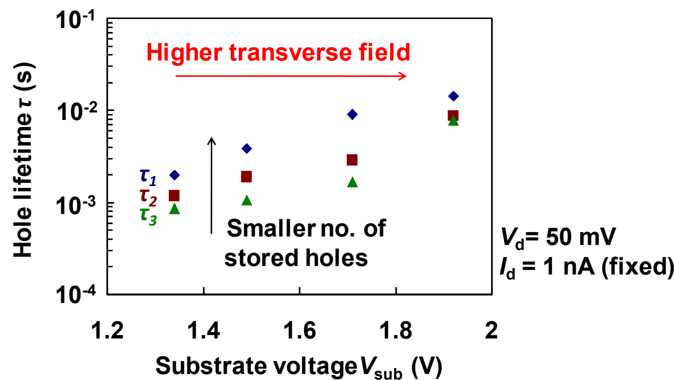

Fig. 8. Hole lifetime as a function of V_{sub}.τ_1, τ_2 and τ_3 are the lifetimes when the number of the stored holes are one, two and three, respectively.

In case of QDFET, the hole lifetime in InAs QDs is longer than a hundred seconds, and a reset gate pulse is necessary for refilling the dots with electrons after illumination [3,4]. In the photo-SET, electron lifetime in the nc-Si dots (detection time) can be as long as 350 s at a specific temperature with the contribution of Si/oxide traps [6]. In the present SOI MOSFET, hole lifetime is much shorter probably due to the bulk defects in the SOI layer as estimated in the previous section, the presence of channel electrons in a short distance, and the lose confinement of holes in the shallow potential well created by the pn junction and gate electric field. The short lifetime is beneficial in that the device does not require reset operation, but there might be some difficulty in controlling the lifetime to an appropriate value. The contribution of the Si/oxide interface traps [6] to the hole lifetime seems to be small considering the fact that the lifetime becomes longer for higher transverse electric field that makes the hole distribution closer to the interface.

It is worthwhile to compare other performance indices of the QDFET and SOI MOSFET. The QE of QDFET is reported to be 0.14% [3] and comparable to 0.15% of the present SOI MOSFET. There are common issues in the small light absorption in thin active layer, and low transmittance of the metallic gate. Higher QE may be attained by the introduction of a resonant cavity structure and more transparent gate material. The dark count rate in the SOI MOSFET is less than 0.2 s^{-1} (no signal in the observation time of 5 s) at 300 K, and this outperforms the 10^{-8} ns^{-1} of the QDFET at 77 K [3], indication the SOI MOSFET is suitable to applications where the photon arrival time is not known.

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3.3. Operation speed

Operation speed of the single-photon detection, i.e. maximum count rate, is limited by the noise and the hole lifetime as described in the Introduction. According to the results in Sections 3.1 and 3.2, the small $|V_{sub}|$ leads to high-speed operation owing to the low noise and short lifetime. It can be seen in Fig. 3 that the minimum noise power for the band width of 5 Hz is 7×10^{-25} A^2 (S_{Id} is 1.4×10^{-25} A^2/Hz). ΔI_d is found to be 29 pA as the peak-to-peak spacing in Fig. 6. If we assume the required SNR of 10 dB (= 3.16), the maximum count rate $(\Delta I_d/SNR)^2/S_{Id}$ becomes 600 s^{-1}. Figure 8 also indicates that the minimum hole lifetime τ_1 of 2×10^{-3} s makes the maximum count rate to be about 500 s^{-1} ($= 1/\tau_1$) to avoid the excessive accumulation of holes. In order to improve these values, ΔI_d could be increased by further down-scaling of the device sizes, and τ_1 could be reduced by introducing defects.

4. Conclusion

Low-frequency current noise in SOI MOSFET was analyzed for photon detection under different V_{sub}'s. It was found that the noise in the SOI MOSFET became low at the transition point between the front- and back-channel operations, and in the back-channel region near the transition point. On both sides, the noise spectra asymptotically approached a single $1/f^2$ line, indicating that the Lorentzian plateau level and time constant increase simultaneously presumably due to the GR processes at bulk defects in the SOI layer. In order to understand the V_{sub} dependence of the hole lifetime, the drain current histograms of the SOI MOSFET were analyzed at different V_{sub}'s and light intensities. It was found that the peaks in the histogram corresponding to the larger number of stored holes became higher as the V_{sub} decreased. This was attributed to the prolonged hole lifetimes caused by the higher electric field inside the body of SOI MOSFET. It can be concluded that, once the inversion channel is induced for detection of the photo-generated holes, the small $|V_{sub}|$ is favorable for short lifetime and low noise, leading to high-speed operation.

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