Enhanced Visible Light Sensitivity by Gold Line-and-Space Grating Gate Electrode in Thin Silicon-On-Insulator p-n Junction Photodiode

メタデータ	言語: eng
	出版者:
	公開日: 2014-11-10
	キーワード (Ja):
	キーワード (En):
	作成者: Satoh, Hiroaki, Ono, Atsushi, Inokawa, Hiroshi
	メールアドレス:
	所属:
URL	http://hdl.handle.net/10297/7959

Enhanced Visible Light Sensitivity by Gold Line-and-Space Grating Gate Electrode in Thin Silicon-On-Insulator p-n Junction Photodiode

Hiroaki Satoh, *Member, IEEE*, Atsushi Ono, and Hiroshi Inokawa, *Member, IEEE*

Abstract— A new type of thin silicon-on-insulator (SOI) p-n junction photodiode (PD) with gold (Au) line-and-space (L/S) grating gate electrode is proposed and demonstrated to have high quantum efficiency (QE) at visible wavelengths. This PD is similar to our previous one in the use of the grating and the metal-oxide-semiconductor (MOS) structure, but is very different in the use of the separate binary grating instead of the continuous one and the thick gate oxide. As a result, the diffracted light from the grating efficiently couples with the lateral propagation mode in the SOI slab waveguide, leading to an external QE one order of magnitude higher than that without the grating. In addition, the importance of the proper setting of the gate and substrate biases is shown so as to realize the wide depletion region and resultant high QE.

Index Terms— metal grating, silicon on insulator technology, photodiode, p-n junction.

I. INTRODUCTION

SILICON-ON-INSULATOR has advantages of high-speed operation and large voltage gain per electric charge for high performance photodetectors because of the low parasitic capacitances. However, due to the small thickness, the sensitivity of SOI photodetector is usually not high. As one approach to solve this problem, the surface plasmon (SP) antenna has been proposed to enhance the infrared light sensitivity of Schottky-junction photodiode (PD) with small volume of silicon (Si) mesa structure [1, 2]. We have also proposed a different kind of SP antenna for visible light detection with gold (Au) line-and-space (L/S) structure that can be applied to SOI metal-oxide-semiconductor (MOS) PD [3]. In this proposed structure, the p-n junction PD was electrically isolated from the metallic antenna by gate silicon dioxide (SiO$_2$), and featured small dark current. In the antenna, a continuous Au L/S grating was used to generate the SP

polariton, thickness of the Au in the space was reduced to about 30 nm to attain light coupling to the underneath Si, and the gate oxide thickness between the antenna and the Si was also reduced to 5 nm to best utilize the near-field light without causing electrical leakage. However, experimentally, the performance of the proposed PD was poor mainly due to the conduction loss of the titanium (Ti) adhesion layer inserted under the Au antenna [4]. Even with a transparent adhesion layer of Si$_3$N$_4$, improvement was still not so high [5], probably due to the insufficient surface quality of the thin Au film.

In this paper, an advanced SOI-MOS PD with Au L/S grating is proposed. The structure appears similar to our previous one [3], but very different in the use of the separate binary grating instead of continuous one and the thick gate oxide, leading to efficient coupling between the diffracted light from the grating and the propagation modes in the SOI slab waveguide. This approach is very similar to the use of a metal grating on a SOI wafer proposed by Crouse et al. [6]. They described that a diffraction mode produced by the grating coupled into a waveguide mode in the top silicon layer of the SOI, with detailed consideration to various resonance mechanisms for enhanced quantum efficiency (QE). Our approach is different in that an insulator is inserted between the grating and the SOI to realize a MOS-type lateral p-n junction PD, and this also leads to better coupling and higher QE than that of Crouse et al.

The spectroscopic QE of the proposed PD is simulated first, the above mentioned mechanism is verified by comparing the theoretical dispersion relationship of the waveguide modes and the grating period-peak wavelength relationship, and the gate oxide thickness is optimized for higher QE. After that, the proposed PD is fabricated, the importance of the proper setting of the gate and substrate biases is noted, and the enhanced light sensitivity is demonstrated and discussed.

II. DEVICE STRUCTURE

Fig. 1 shows the proposed SOI-MOS p-n PD with separate Au L/S grating. The grating is more easily to be fabricated due to the one Au thickness, as opposed to the two different thicknesses in the previous structure [3]. The adverse effect of Ti adhesion layer was minimized, since it only exists under the
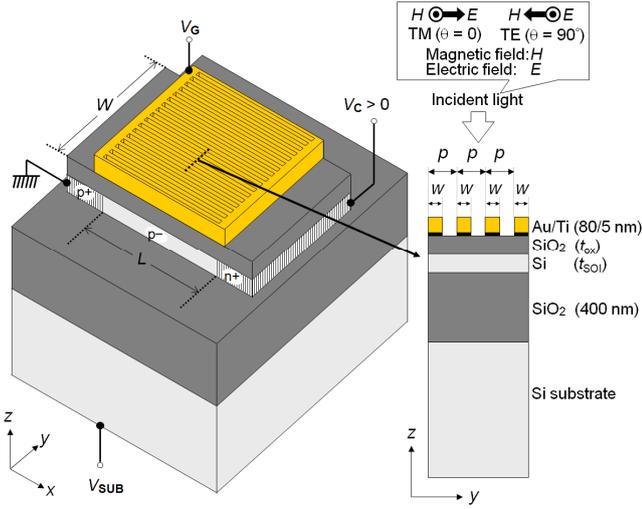
Fig. 1. Device structure of proposed SOI-MOS p-n photodiode with metal Au L/S grating gate electrode and definition of incident light polarization with respect to grating direction.

TABLE I
MATERIAL PARAMETERS OF METALS FOR 2D FDTD CALCULATIONS [8]

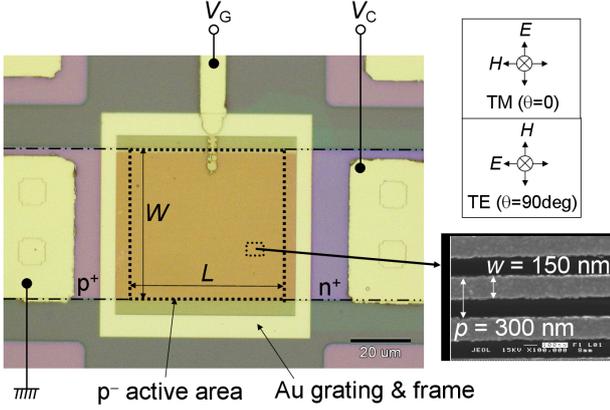|	Au	Ti
ω_p (rad/s)	1.372×10^{16}	1.108×10^{14}
f_0	0.76	0.148
Γ_0 (rad/s)	8.052×10^{13}	1.246×10^{14}
k	5	4
f_1	0.024	0.899
ω_1 (rad/s)	6.304×10^{14}	1.180×10^{15}
Γ_1 (rad/s)	3.661×10^{14}	3.458×10^{15}
f_2	0.01	0.393
ω_2 (rad/s)	1.261×10^{15}	2.347×10^{15}
Γ_2 (rad/s)	5.242×10^{14}	3.826×10^{15}
f_3	0.071	0.187
ω_3 (rad/s)	4.511×10^{15}	3.812×10^{15}
Γ_3 (rad/s)	1.322×10^{15}	2.527×10^{15}
f_4	0.601	0.001
ω_4 (rad/s)	6.539×10^{15}	2.952×10^{16}
Γ_4 (rad/s)	3.789×10^{13}	2.677×10^{15}
f_5	4.384	
ω_5 (rad/s)	2.024×10^{16}	
Γ_5 (rad/s)	3.364×10^{15}	

Fig. 2. Top view of the fabricated SOI-MOS p-n photodiode with Au L/S grating. The polarizations with respect to the direction of Au L/S grating are also shown. Au grating is surrounded by a frame to be used as a gate electrode. Dimensions of the p⁻ active area are $L = 50$ μm and $W = 50$ μm.

Au line. This PD can be fabricated by the following steps. At first, the SOI thickness (t_{SOI}) of a commercial p-type SOI wafer is adjusted by oxidization and etching of Si. The initial impurity (boron) concentrations in the SOI and the substrate are both 1×10^{15} cm⁻³. In the second step, the SOI pattern with a width of W is delineated by photolithography and Si etching. Thirdly, boron fluoride (BF_2^+) and arsenic (As^+) ions are implanted to the anode and cathode regions of the SOI, respectively. Then, the thick gate oxide on the SOI layer with the thickness (t_{ox}) is formed by oxidization of the SOI layer and SiO₂ deposition, and the contact holes are opened. Finally, the L/S grating and probing pads are formed by electron beam (EB) lithography, Ti and Au evaporations, and liftoff. The gate oxide thickness is much larger than that of our previous structures [3] because of the different mechanism of the light coupling. The incident light enters normally to the PD surface. In this paper, the incident light is called transverse magnetic (TM)-polarized light when the L/S direction and magnetic field component coincide, and is called transverse electric (TE)-polarized light when the L/S direction and electric field component coincide.

Fig. 2 shows the top view of the one of the fabricated devices with p⁻ active area of $L = W = 50$ μm, and scanning electron microscopy (SEM) image of the grating with the period $p = 300$ nm and the line width $w = 150$ nm. Au L/S grating has a frame to obtain electrical contact as a gate electrode. The polarizations (TM and TE) with respect to the direction of Au L/S grating are also shown in Fig. 2.

III. DEVICE DESIGN BY FDTD CALCULATIONS

A. Conditions for FDTD Calculations

In order to optimize the structure for high light sensitivity, we perform the two-dimensional (2D) finite difference time domain (FDTD) calculation [7] of our proposed SOI-MOS PD. To simplify the calculations, a unit periodic structure with grating period p is assumed as shown in Fig. 1. The boundary conditions for computational space in y-, and z-directions are periodic boundary, and absorbing boundary with the perfectly matched layer (PML) [8], respectively. The discretized interval and time step are $\Delta d\ (= \Delta y = \Delta z) = 1$ nm and $\Delta t = \Delta d/(2c_0) = 1.67 \times 10^{-18}$ s, respectively. Here, c_0 is the light speed in vacuum.

In this paper, the complex relative permittivities with wavelength-dispersion for the metals of Au and Ti are expressed by the Lorentz-Drude oscillator model as follows:

$$\varepsilon_r(\omega) = 1 - \frac{f_0 \omega_p^2}{\omega(\omega - i\Gamma_0)} + \sum_{j=1}^{k} \frac{f_j \omega_p^2}{(\omega_j^2 - \omega^2) + i\omega\Gamma_j}, \qquad (1)$$

where ω is the angular frequency for incident light, ω_p is the plasma frequency, k is the number of oscillators with frequency ω_j, strength f_j, and damping constant Γ_j. In (1), the first and the second terms are based on Drude model formulation, and the third term is multi-pole Lorentz model formulation. The Si and Ti parameters in this paper are summarized in Table 1 [9]. As our measured results shown below, these Au and Ti parameters are very useful for wide optical wavelength range. The
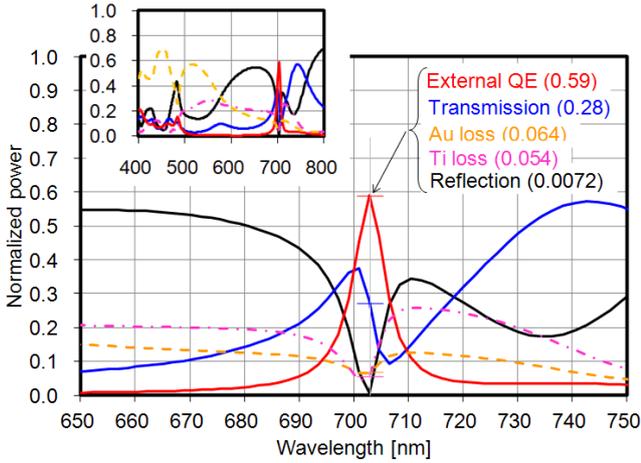
Fig. 3. Spectroscopic response of the optical power components in SOI PD with Au L/S grating. Incident light is TM-polarized. Gate oxide and SOI thicknesses are t_{ox} = 100 nm and t_{SOI} = 100 nm, respectively. Duty ratio of Au L/S grating is fixed at w/p = 0.5. Inserted figure shows spectroscopic responses for wider wavelength range. Transmission is for the power entering the Si substrate.

complex relative permittivity with wavelength-dispersion for Si is expressed by the single-pole Lorentz model formulation as follows:

$$\varepsilon_r(\omega) = \varepsilon_\infty + \frac{(\varepsilon_s - \varepsilon_\infty)\omega_p^2}{\omega_p^2 + 2i\omega\Gamma - \omega^2}, \qquad (2)$$

where ε_∞ is the relative permittivity at infinite frequency, and ε_s is the static or zero-frequency relative permittivity. ω_p is the frequency of pole pair, and Γ is the damping coefficient. The Si parameters, ε_s = 12.7, ε_∞ = 8.3, ω_p = 5.145 × 10^{15} rad/s, and Γ = 5.145 × 10^{13} rad/s, are obtained by fitting the experimental results of SOPRALAB [10]. Moreover, the relative permittivities for SiO$_2$ and vacuum are ε_r = 2.13 and 1, respectively, which are independent of the wavelength [3]. The relative permeability μ_r of all the materials is assumed to be unity.

The external QE, that is equivalent to the absorption efficiency in the SOI layer, can be predicted by subtracting the output power from the input power along the SOI boundaries, if the photogenerated carriers contribute to the photocurrents perfectly. The frequency (wavelength) response is obtained by performing the fast Fourier transformation (FFT) to the results of the Gaussian pulse response in 2^{19} sampling time steps of the FDTD calculations.

B. Design and Structural Optimization for Proposed SOI-MOS PD

In this section, spectroscopic QE is calculated to discuss the operation mechanism of the proposed PD. Primarily, the grating pitch dependence is evaluated to in conjunction with the waveguide modes in the SOI. Since the unique feature of the proposed PD is that the grating is separated from SOI by the gate oxide, its thickness is optimized while the thicknesses of SOI, buried oxide (BOX) layer underneath the SOI, Au, and Ti are fixed at t_{SOI} = 100 nm, t_{BOX} = 400 nm, t_{Au} = 80 nm, and t_{Ti} =
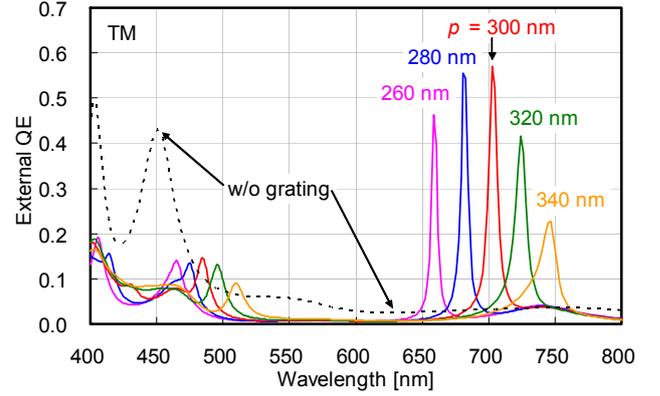
(a)
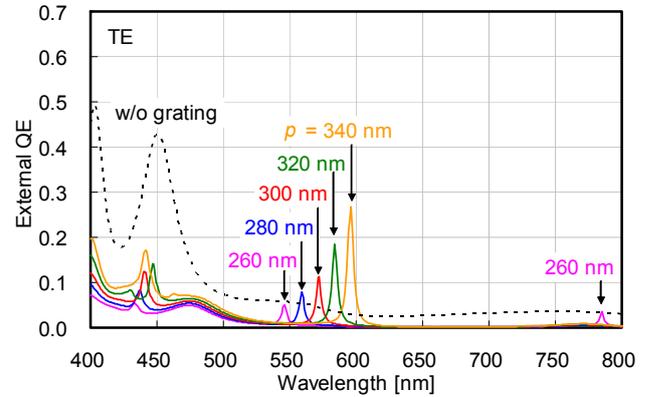
(b)

Fig. 4. Calculated spectroscopic external quantum efficiency (QE) for (a) TM- and (b) TE- polarized lights. Gate oxide and SOI thicknesses are t_{ox} = 100 nm and t_{SOI} = 100 nm, respectively. Duty ratio of Au L/S grating is fixed at w/p = 0.5.

5 nm.

The importance of the Au thickness optimization was pointed out by Crouse et al. [6] from the view point of the vertical surface resonance (VSR). Our calculation revealed that the QE was maximized in the sub-resonance region at t_{Au} = 80 nm, although a slightly lower resonance peak could be found at 370 nm (data not shown).

The optimization of the BOX thickness is also very important as was pointed out by Crouse et al. [6] since the proper choice at around the quarter wavelength results in reduced transmission and increased coupling to the SOI. The FDTD calculation revealed that the maximum QE could be found at t_{BOX} = 200, 440... nm for the present structure (data not shown). This time, the use of a commercial SOI with t_{BOX} = 400 nm only reduced the QE from 62 to 59%, and is acceptable, but t_{BOX} may have to be customized depending on the target wavelength. Also note that the optimized t_{BOX} of 200 nm is away from the quarter wavelength of 120 nm, suggesting that more detailed interpretation is necessary.

In addition, the duty ratio of L/S grating is also fixed at w/p = 0.5. We choose this duty ratio for easier fabrication of L/S grating, although the QE peaks broadly at w/p = 0.7.

In the FDTD calculations, all the components of response in our proposed device, such as external QE, reflection, transmission, Au loss, and Ti loss can be obtained [5]. Transmission is defined for the power component passing through the top boundary of the Si substrate, and the power component is eventually absorbed in the Si substrate and the PML absorber at the bottom boundary. For example, the spectroscopic optical response of perfectly periodic structure for TM-polarized light is shown in Fig. 3, when $p = 300$ nm and $t_{ox} = 100$ nm. Very sharp peak with high external QE appears can be obtained at the wavelength of 703 nm. The other components are significantly reduced only at the wavelength. Here, the grating period dependence of external QE for the range from $p = 260$ nm to 340 nm is considered as shown in Fig. 4. This figure includes the result without the grating. Sharp peaks of external QE exist at the different wavelength range for each polarized light. It is also shown that the main peak wavelength can be controlled by the grating period for both polarized lights. Especially for TM-polarized light, the main peak values of external QE are larger than those of our conventional SOI-MOS PD [3]-[5]. When $p = 300$ nm and TM-polarized light incidence, the enhancement factor, ratio of QEs with and without Au L/S grating, reaches as high as 18 at the wavelength of 703 nm.

Such enhancement of external QE by Au L/S grating is caused mainly by coupling between the diffracted light from Au L/S grating and the SOI waveguiding mode. In order to analyze the coupling, the dispersion relation for the symmetrical slab waveguide with 100-nm-thickness Si core and infinite-thickness SiO$_2$ claddings is estimated by the following transcendental equations [11].

$$\begin{cases} \tan\left(\dfrac{ht_{core}}{2} - m\dfrac{\pi}{2} \right) = \dfrac{\sqrt{V^2 - h^2 t_{core}^2}}{ht_{core}} \\ \qquad\qquad\qquad (m = 0, 1, 2, \cdots, \text{TE wave}) \\ \tan\left(\dfrac{ht_{core}}{2} - m\dfrac{\pi}{2} \right) = \dfrac{n_{core}^2}{n_{clad}^2} \dfrac{\sqrt{V^2 - h^2 t_{core}^2}}{ht_{core}} \\ \qquad\qquad\qquad (m = 0, 1, 2, \cdots, \text{TM wave}) \end{cases} \quad (3)$$

where

$$h = \sqrt{\left(\frac{2\pi n_{core}}{\lambda} \right)^2 - \left(\frac{2\pi}{\lambda_g} \right)^2}, \quad V = \frac{2\pi}{\lambda} t_{core} \sqrt{n_{core}^2 - n_{clad}^2},$$

t_{core} is core thickness, and n_{core} and n_{clad} are refractive indices for core and cladding, respectively. λ_g is propagation wavelength in core. The refractive indices for core and cladding are set by the permittivities for Si and SiO$_2$, respectively, as mentioned above. The comparison between the dispersion relation of the symmetrical slab waveguide with 100–nm-thick Si core and infinite-thick SiO$_2$ claddings (lower and left axes) and the peak wavelength of each period (upper and right axes) is shown in Fig. 5. By plotting the peak wavelengths of external QE as a function of the grating period p, we can see that the peak positions coincide with the dispersion relation for each waveguiding mode. As a results, the sharp peak with high QE appears when the guided wavelength is nearly equal to the
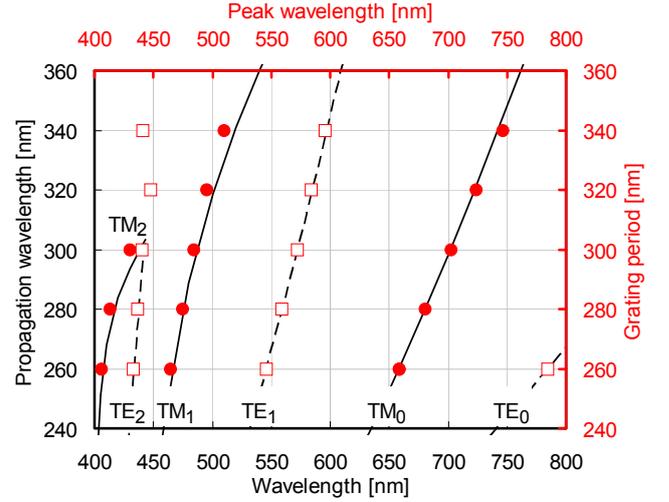

Fig. 5. Comparison between relationships of peak wavelengths of calculated external quantum efficiency (QE) vs. grating period p in Fig. 3 (circles and rectangles, upper and right axes), and the propagation wavelengths of lateral waveguide modes in SOI layer vs. free-space wavelength (solid and dotted lines, lower and left axes). Propagation wavelengths are obtained by solving Eq. (3) for symmetrical slab waveguide composed of 100-nm-thick Si core and infinite-thick SiO$_2$ claddings [11].
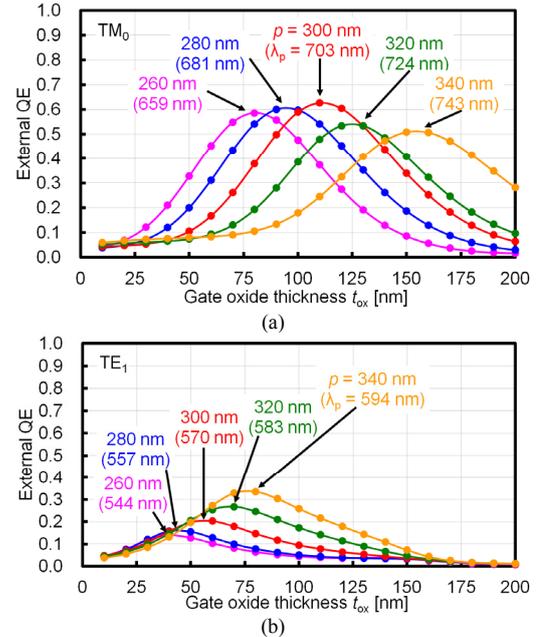

Fig. 6. Calculated peak external quantum efficiencies (QE) as a function of gate oxide thickness with various grating periods p (corresponding to peak wavelengths λ_p) for (a) TM- and (b) TE-polarized lights. SOI thickness is $t_{SOI} = 100$ nm. Duty ratio of Au L/S grating is fixed at $w/p = 0.5$.

grating period. Thus, the enhancement of external QE by Au L/S grating is caused mainly by the coupling between the diffracted light from Au L/S grating and the lateral propagation mode in the SOI waveguide. Applying this relationship, the peak wavelength can be estimated for various grating periods and SOI thicknesses. In the design for our proposed SOI-MOS PD, one more important parameter is the gate oxide thickness (t_{ox}), because the external QEs are sensitive for this parameter. Fig. 6 shows external QEs with respect to gate oxide thickness t_{ox} for each incident polarization and each grating period. The
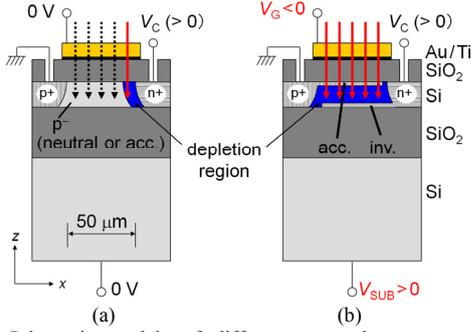
Fig. 7. Schematic models of different external quantum efficiencies depending on conditions of depletion region. Solid and dotted arrows indicate detectable and undetectable light rays, respectively, due to position and volume of depletion region. "acc." and "inv." represent "accumulated" and "inverted", respectively.

optimized gate oxide thickness exists individually for each grating period corresponding to the peak wavelength, because there is optimal coupling efficiency between the diffracted light and the waveguiding light for each grating period. For the grating period range studied this time, the optimized gate oxide thicknesses are much larger than that of our previous structures [3].

IV. Measured External Quantum Efficiency and Discussions

A. Gate and Substrate Bias Dependences

Since this grating is surrounded by a frame, all the gold lines of the grating are connected electrically. Thus, this grating can work as gate electrode for biasing the entire light sensitive area i.e. p⁻ Si area. By applying bias voltages to this gate and the substrate electrodes, the position and the volume of the depletion region can be controlled to maximize the external QE. The schematic models are shown in Fig. 7. If no biases are applied for neutral condition, carrier distribution is expected as shown in Fig. 7 (a). In this case, the external QE becomes low due to the small volume of depletion region in the p⁻ active area. On the other hand, when appropriate bias voltages are applied to these two electrodes, the volume of depletion region and external QE can be maximized as shown in Fig. 7 (b). In this example, top Si area at the gate oxide/SOI interface is accumulated ("acc." in Fig. 5) by the negative bias voltage applied to the gate electrode, and bottom Si area at the SOI/BOX interface is inverted ("inv.") by the positive bias voltage applied to the substrate electrode. When the top Si area is inverted and the bottom Si area is accumulated, the external QE can be also maximized. In the later two cases with large QE, the electric field in the depletion region becomes vertical, and the carrier transit time becomes smaller due to the small thickness of the SOI. However, the operation speed is then limited by the large depletion layer capacitance and the series resistances of the inversion and accumulation layers.

Fig. 8 shows the measured dark current and the external QE as a function of substrate voltage V_{SUB} with various gate voltages V_G for 680-nm-wavelength and TM-polarized light where the fabricated PD can attain the maximum external QE.
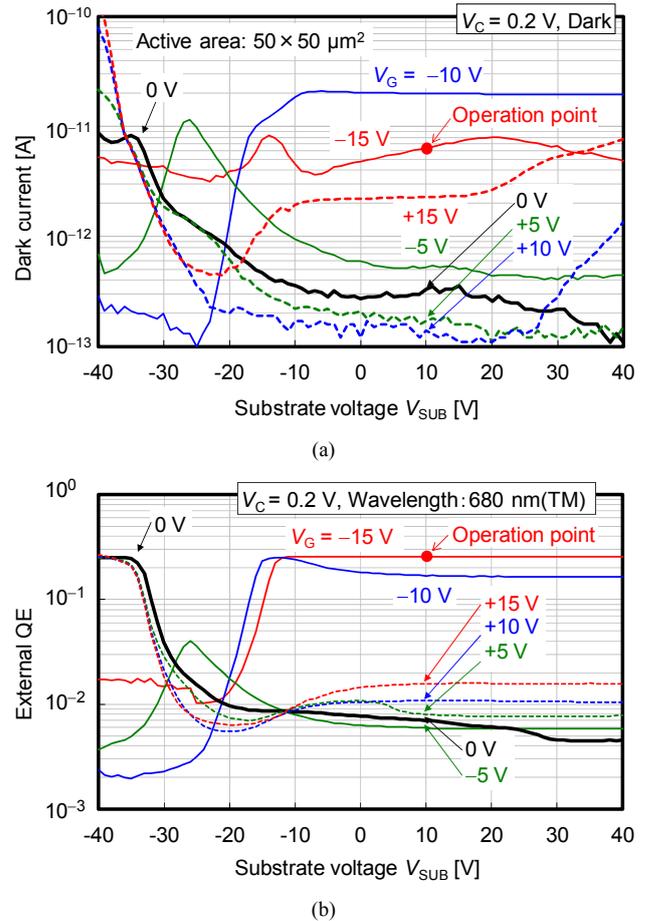

(a)

(b)

Fig. 8. (a) Measured dark current and (b) external quantum efficiency (QE) as a function of substrate voltage V_{SUB} for various gate voltages V_G. Gate oxide and SOI thicknesses of fabricated device are t_{ox} = 100 nm and t_{SOI} = 95 nm, respectively. Grating period is p = 300 nm, and duty ratio is w/p = 0.5. In (b), the wavelength and the polarization of incident light are 680 nm and TM (θ = 0), respectively. The cathode voltage V_C is fixed at 0.2 V.

The dark current seems to reflect the volume of the depletion region, and also to be affected by the high electric field between the accumulation layer and the n⁺ cathode, and the inversion layer and the p⁺ anode. In the calculation of the external QE, the dark current is subtracted from the current under the illumination to obtain the net photo-current.

When the gate voltage is V_G = -15V, for example, the maximum external QE of 25 % can be obtained in the region of the substrate voltage V_{SUB} from -10 V to 40 V. Also, when the gate voltage V_G is from 0 V to +15 V, the maximum external QE can be obtained near V_{SUB} = -40 V. The neutral point is shifted to around V_{SUB} = -22 V probably due to the unexpected charging effect during the fabrication process. Based on the results, the bias voltages of V_G = -15V and V_{SUB} = +10 V are used hereafter.

B. Spectroscopic External Efficiencies for TM- and TE-Polarized Lights

Fig. 9 shows the spectroscopic external QE for (a) TM- and (b) TE-polarized lights. In the case without Au L/S grating, there is a peak with relatively high external QE at the wavelength of 435 nm due to the high absorption coefficient of
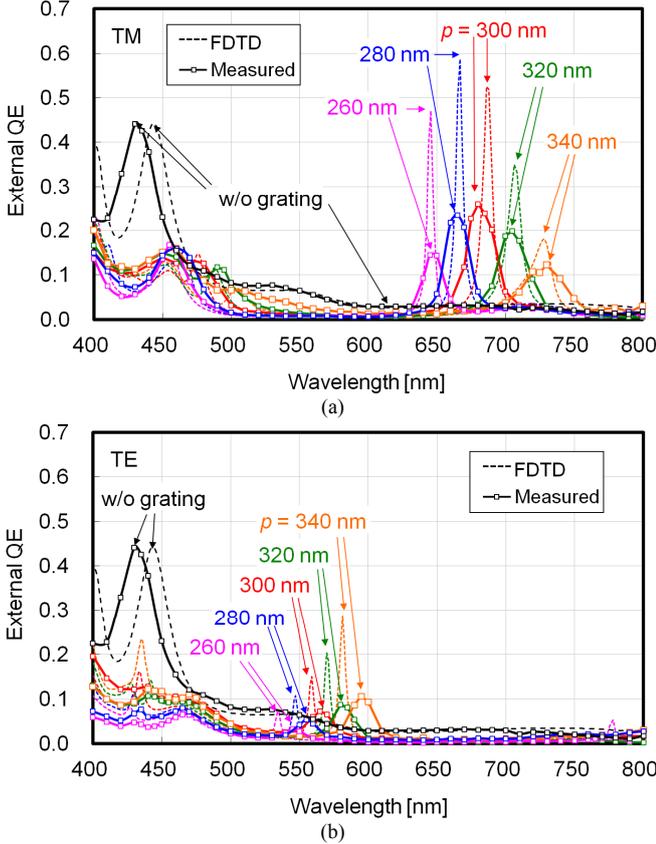
Fig. 9. Measured (solid lines) and calculated (dotted lines) spectroscopic external quantum efficiency (QE) for (a) TM- and (b) TE- polarized lights. Gate oxide and SOI thicknesses of fabricated device are t_{ox} = 100 nm and t_{SOI} = 95 nm, respectively. Duty ratio of Au L/S grating is fixed at w/p = 0.5. In the case with Au L/S grating, bias voltages are fixed at V_C = 0.2 V, V_G = 15 V, and V_{SUB} = 10 V. In the case without grating, bias voltages are fixed at V_C = 0.2 V, and V_{SUB} = -40 V.

Si for shorter wavelength region and the interferences in the multilayered structure. However, the external QE becomes small in the wavelength range longer than 500 nm. With Au L/S grating, the enhancement effects can be observed in the wavelength range from 650 nm to 750 nm for TM-polarized light, and from 560 nm to 600 nm for TE-polarized light. Especially, the external QE reaches as high as 25 % at the wavelength of 680 nm for TM-polarized light, when the grating period is p = 300 nm. In this case, the enhancement factor is 8.2.

Moreover, these peak wavelengths for both polarized lights can be controlled by the grating period p. Such property is caused by the coupling between the diffracted light from the Au L/S grating and the SOI waveguiding mode. Thus, the peak wavelengths for TM- and TE-polarized lights are different even for the same grating period p as explained previously.

C. Polarization Angle Dependence

Fig. 10 shows the external QE as a function of the polarization angle of incident light at the wavelength of 680 nm. This is the peak wavelength for TM-polarized light when p = 300 nm. The PD without Au L/S grating does not show polarization dependence. On the other hand, the polarization dependence can be observed with the Au L/S grating. The
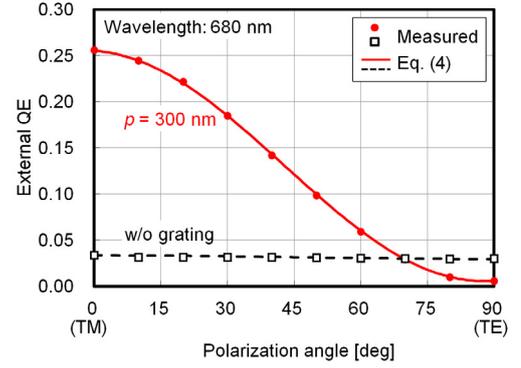

Fig. 10. Dependence of external quantum efficiency (QE) on polarization angle. Fitting curve is based on Eq. (4). Gate oxide and SOI thicknesses of fabricated device are t_{ox} = 100 nm and t_{SOI} = 95 nm, respectively. Grating period is p = 300 nm, and duty ratio is w/p = 0.5. In the case with Au L/S grating, bias voltages are fixed at V_C = 0.2 V, V_G = -15 V, and V_{SUB} = 10 V. In the case without grating, bias voltages are fixed at V_C = 0.2 V, and V_{SUB} = -40 V.

external QE is enhanced by Au L/S grating in the polarization angle range from 0 to 70 deg. In this case, the rejection ratio for TE-polarized light reaches 46. If the external QEs for TM- and TE-polarized lights (η_{TM} and η_{TE}, respectively) are known, the polarization angle dependence of external QE can be obtained by the following equation,

$$\eta(\lambda,\theta) = \eta_{TE}(\lambda)\sin^2\theta + \eta_{TM}(\lambda)\cos^2\theta \ . \tag{4}$$

The fitting curve is drawn by substituting the measured external QEs for TM- and TE-polarized lights corresponding to the polarization angles θ = 0 and 90 deg, respectively, in Fig. 10. The measured external QEs are almost on the fitting curve. In addition, from the measured external QEs at θ = 0 and 90 deg, the one for randomly polarized light can be estimated from the following formulation.

$$\eta_{random}(\lambda) = \frac{1}{\pi/2}\int_0^{\pi/2}\eta(\lambda,\theta)d\theta = \frac{1}{2}\{\eta_{TE}(\lambda) + \eta_{TM}(\lambda)\} . \tag{5}$$

In the case of our fabricated PD with p = 300 nm, the external QE of 13.1 % for randomly polarized light at the wavelength of 680 nm can be expected from the measured results in Fig. 9.

V. CONCLUSION

A new type of SOI-MOS PD with separate Au L/S grating and thick gate oxide was proposed, which realized remarkable enhancement in sensitivity even for thin SOI layer, and featured wavelength and polarization selectivities. The enhancement of external QE could be obtained mainly by the efficient coupling between the diffracted light from Au L/S grating and the lateral propagation mode in the SOI waveguide, as was manifested by the fact that the grating period-peak wavelength relationship coincided well with the theoretical dispersion (propagation and free-space wavelengths) relationship of the SOI slab waveguide modes. Experimentally, it was demonstrated that external QE as high as 25 % could be attained with 95-nm-thick Si layer at the wavelength of 680 nm for TM-polarized light. In addition, it was found that the negative gate bias to accumulate the top Si surface and positive substrate bias to invert the bottom Si surface, and vice versa, were necessary to realize the

wide depletion region and resultant high QE, and the polarization angle dependence of the QE could be reproduced by summing the respective responses for TM and TE components of the incident light [as described in (4)]. Considering the enhanced sensitivity and unique features described above, the proposed PD would be of great use especially when it is integrated with advanced SOI-based LSIs.

REFERENCES

[1] T. Ishi, J. Fujikata, K. Makita, T. Baba, and K. Ohashi, "Si nano-photodiode with a surface plasmon antenna," Jpn. J. Appl. Phys., vol. 44, no. 12 pp. L364-L366, Mar. 2005.

[2] D. Okamoto, J. Fujikata, K. Nishi, and K. Ohashi, "Numerical study of near-infrared photodetectors with surface-plasmon antenna for optical communication," Jpn. J. Appl. Phys., vol. 47, no. 4, pp. 2921-2923, Apr. 2008.

[3] H. Satoh, and H. Inokawa, "Surface plasmon antenna with gold line and space grating for enhanced visible light detection by a silicon-on-insulator metal–oxide–semiconductor photodiode, " IEEE Trans. Nanotechnology, vol. 11, no. 2, pp. 346-351, Mar., 2012.

[4] H. Satoh, and H. Inokawa, "Spectroscopic response of SOI photodiode with gold line-and-space surface plasmon antenna," in Proc. Silicon Nanoelectronics Workshop, 2009, pp. 117-118.

[5] H. Satoh, Y. Matsuo, H. Inokawa, and A. Ono, "Investigation of adhesion materials for gold line-and-space surface plasmon antenna on SOI-MOS photodiode," Advanced Materials Research, vol. 222, pp. 201-204, Apr. 2011.

[6] D. Crouse, and P. Keshavareddy, "A method for designing electromagnetic resonance enhanced silicon-on-insulator metal-semiconductor-metal photodetectors," J. Opt. A: Pure Appl. Opt., vol. 8, no. 2, pp. 175-181, Jan. 2006.

[7] A. Taflove and S. C. Hagness, Computational Electrodynamics—The Finite Difference-Time Domain Method, 3rd ed., MA: Artech House, 2005.

[8] J.-P. Berenger, "A perfectly matched layer for the absorption of electromagnetic waves," J. Computational Physics, vol. 114, no. 2, pp. 185-200, Oct. 1994.

[9] A. D. Rakic, A. B. Djurisic, J. M. Elazar, and M. L. Majewski, "Optical properties of metallic films for vertical cavity optoelectronic devices," Applied Optics, vol. 37, no. 22, pp. 5271-5284, Aug. 1998.

[10] (1998). http://www.sopra-sa.com/index.php

[11] J. M. Liu, Photonic Devices, Cambridge University Press, pp. 95-99, 2005.

Hiroaki Satoh (S'01-M'04) received the Ph.D degree from Hokkaido University, Sapporo, Japan, in 2004.

He became an Assistant Professor with the Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan, in 2007.

Atsushi Ono received Ph.D degree in applied physics from Osaka University, Osaka, Japan, in 2006, respectively.

Since 2009, he has been an Assistant Professor of tenure track with the Division of Global Research Leaders, Shizuoka University, Hamamatsu, Japan.

Hiroshi Inokawa (M'90) received the Ph.D. degree in electrical engineering from Kyoto University, Kyoto, Japan, in 1985.

In 2006, he became a Professor of the Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan.