Foreword

THIS Special Issue of the IEEE TRANSACTIONS ON NANOTECHNOLOGY is devoted to papers from the 2005 Silicon Nanoelectronics Workshop, the tenth workshop in the series, which was held on June 12–13, 2005, at Rihga Royal Hotel, Kyoto, Japan. The workshop shed light on all aspects of silicon-based nanoelectronics, including physics of nanostructures, multiple gate MOSFETs, gate stack engineering, quantum/CMOS hybrid architectures, single electron devices, novel nanoscale device technologies, and nanoscale memories. This workshop was the largest so far, with 181 in attendance from all over the world. There were 5 invited talks, which covered a wide area from nanoscale architectures to spintronic devices, 21 contributed talks, and 46 poster presentations. There was also a rump session, "Silicon Nanoelectronics: 10 Years Ago and 10 Years Ahead," moderated by Hiroshi Mizuta (Tokyo Institute of Technology) and Sung Woo Hwang (Korea University).

We would like to thank the Technical Program Committee members, Asen Asenov (University of Glasgow), Simon Deleonibus (LETI), David K. Ferry (Arizona State University), David J. Frank (IBM), Toshiro Hiramoto (University of Tokyo), Sung Woo Hwang (Korea University), Tsu Jae King (University of California, Berkeley), Seiichi Miyazaki (Hiroshima University), Hiroshi Mizuta (Tokyo Institute of Technology), Yukinori Ono (NTT), Donggun Park (Samsung), Wolfgang Porod (Notre Dame University), Nobuyuki Sano (Tsukuba University), Shigeo Satoh (Fujitsu), Thomas Skotnicki (STMicroelectronics), Eiichi Suzuki (AIST), Ken Uchida (Toshiba), and Hitoshi Wakabayashi (NEC), for their efforts in making the workshop successful and attractive. We would also like to thank the many reviewers who ensured the quality of this Special Issue. Finally, we would like to thank the Japan Society of Applied Physics for its support of the workshop. The next Silicon Nanoelectronics Workshop will be held on June 11–12, 2006, in Hawaii.

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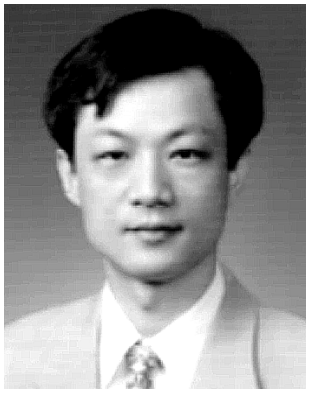
Michiharu Tabe received the B.S., M.S., and Dr.Eng. degrees from Keio University, Japan, in 1973, 1975, and 1984, respectively.

From 1975 to 1994, he worked at Nippon Telegraph and Telephone (NTT) Corporation Laboratories, Atsugi, Japan, in the research field of surface-related Si processes for advanced MOS and bipolar transistors and also in Si nanodevices such as single-electron devices. During his work at NTT, from 1984 to 1985, he was with Stanford University as a Visiting Researchcher, working on synchrotron radiation for characterization of ultrathin gate oxides. In 1994, he joined the Research Institute of Electronics, Shizuoka University, Japan, as a Professor. His current research interests include Si single-electron devices, Si tunneling devices, self-organization phenomena, and their application to photonic devices.

Dr. Tabe served as the General Chair of the Silicon Nanoelectronics Workshop, in 2005, and the Program Chair, in 2003. He also served as the Program Committee Chair of the 12th International Conference on Solid Films and Surfaces, in 2004.



Byung-Gook Park (M'90) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1990.

From 1990 to 1993, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he contributed to the development of 0.1-μm CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments Incorporated, Dallas, TX, where he developed 0.25-μm CMOS. In 1994, he joined the School of Electrical Engineering, Seoul National University, as an Assistant Professor, where he has been a Professor since 2004. His current research interests are nanoscale CMOS devices, Si single-electron devices, organic electroluminescent display, and nonvolatile memory devices.

Dr. Park was a member of the IEEE Electron Devices Society International Electron Devices Meeting (IEDM) Subcommittee on Solid-State Devices from 2001 to 2002.