A Multiple-Valued Logic and Memory With Combined Single-Electron and Metal–Oxide–Semiconductor Transistors

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***Abstract*—Devices that combine single-electron and metal–oxide–semiconductor (MOS) transistors are newly proposed as basic components of multiple-valued (MV) logic, such as a universal literal gate and a quantizer. We verified their operation using single-electron and MOS transistors fabricated on the same wafer by pattern-dependent oxidation of silicon. We also discuss their application to an analog-to-digital converter, a MV adder, and MV static random-access memory.**

***Index Terms*—Literal gate, MOSFET, multiple-valued logic, multiple-valued memory, quantizer, single-electron transistor (SET).**

I. Introduction

ADVANCES in large-scale integrated circuits (LSIs) have been based mostly on binary logic, and some research on emerging single-electron devices (SEDs) has followed the same path [1]–[5]. However, the problems in present LSI technology, such as increased interconnect delay and power consumption [6], [7], cannot be solved by simply replacing conventional devices with SEDs, or it may even get worse due to the low drivability originating from the high tunneling resistance and the high off-state leakage related to the low charging energy in the present technology [2], [3]. An advanced logic scheme that achieves higher functionality with fewer components and interconnections, is thus very desirable for SEDs. Multiple-valued (MV) logic is recognized as an advanced logic scheme in this sense [8]–[12], but its implementation has been limited to conventional devices, which are inherently single-threshold or single-peak and thus not fully suited for MV logic. In contrast, SEDs are very suitable for MV logic because the discreteness of the electronic charge in the Coulomb island can be directly related to multiple-valued operation. Actually, some single-electron MV logics have been proposed [13], [14], but the MV operation has not yet been verified experimentally mainly because the schemes require unrealistic accuracy or limitations with respect to device parameters and operating conditions.

For the same reason, SEDs are also very suitable for MV memory. Unlike MV logics, MV schemes are already practically used in MOS read-only [12] and flash memories [15], [16]. Floating-node-type memories with SEDs have also been demonstrated experimentally [17], [18]. However, static memory, which features a fast simple write operation and stable retention while the power is on, has not practically been achieved with SEDs. A bistable flip-flop (inverter string) has been proposed [2], but it would be difficult to develop it into a MV memory. Preliminary results on a MV memory have been reported recently by us [19], but they were only for a slow and complex current sweep measurement.

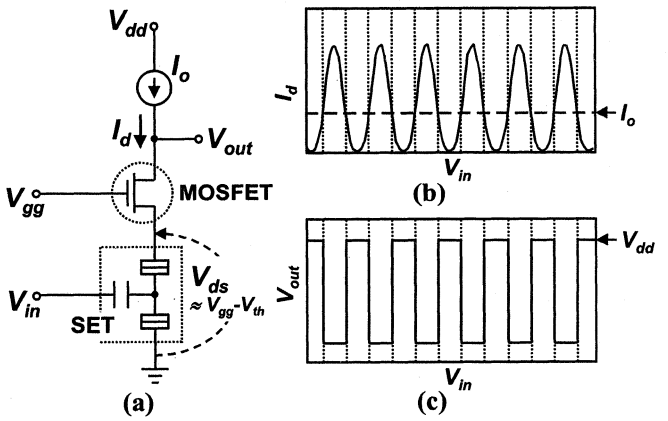

Fig. 1. (a) Schematic of the universal literal gate comprising a SET, a MOSFET and a constant-current (CC) load I_o. (b) I_d–V_{in} characteristics, which are almost completely independent of V_{out} since the V_{ds} of the SET is kept nearly constant at V_{gg} minus V_{th}, the threshold voltage of the MOSFET. (c) Expected transfer (V_{in}–V_{out}) characteristics.

In this paper, we introduce a series of single-electron MV logic and memory, in which MOSFETs supplement single-electron transistors (SETs) to attain practical characteristics. We demonstrate the operation of basic components of MV logic, such as a universal literal gate and a quantizer, which is equivalent to a MV static memory, using devices fabricated by the Si-based pattern-dependent oxidation (PADOX) process [20], [21]. The usefulness of the proposed single-electron MV logic and memory is discussed using an analog-to-digital converter (ADC), a MV adder, and MV static random-access memory (SRAM) as examples.

II. Operation Principle

A universal literal gate is a basic component of the MV logic. Since it converts a MV input to a periodic binary output, a SET, which has periodic I_d–V_{gs} characteristics, is readily applicable. However, a SET has disadvantages as a circuit element. The drain current heavily depends on the drain voltage, and thus the output resistance is low. The maximum voltage gain of a simple inverter, C_g/C_d, where C_g is the gate capacitance and C_d is the drain capacitance, is very small, usually less than one

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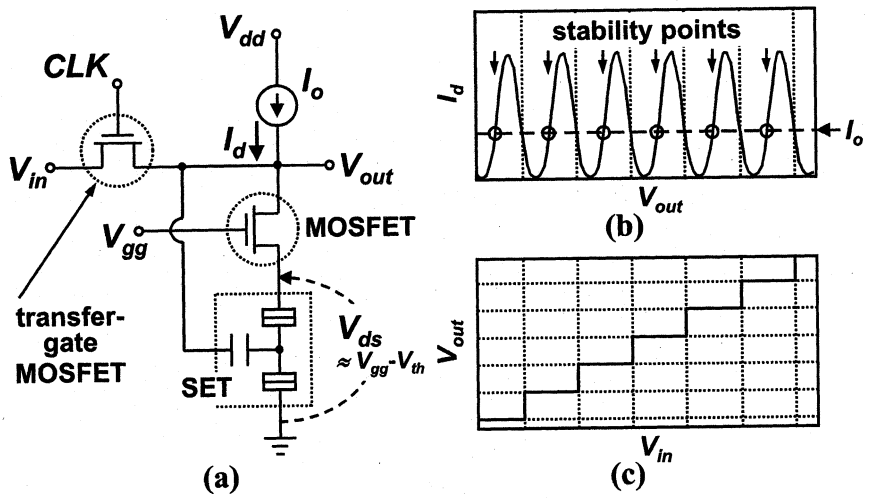


Fig. 2. (a) Schematic of the proposed quantizer (static memory). (b) Two-terminal I_d–V_{out} characteristics of the SET-MOSFET device with the SET gate shorted to the MOSFET drain. (c) Expected transfer (V_{in}–V_{out}) characteristics. V_{in} is transferred to V_{out} through the transfer gate MOSFET and is quantized to a stability point after the gate is cut off.

or a little more than one. Applicable drain voltage is also limited to a small value, e/C_Σ, where e is an electronic charge and C_Σ is the total capacitance around the Coulomb island, to sustain the Coulomb-blockade condition. In order to overcome these disadvantages and to make a practical MV logic, we constructed a hybrid circuit containing MOSFETs. Fig. 1(a) is a schematic of the universal literal gate comprising a SET, a MOSFET and a constant-current (CC) load I_o. A MOSFET with a fixed gate bias of V_{gg} is used here to keep the SET drain voltage almost constant at V_{gg}–V_{th}, where V_{th} is the MOSFET threshold voltage. This V_{gg}–V_{th} is set low enough to sustain the Coulomb-blockade condition. Current through this circuit increases and decreases periodically as a function of input voltage [Fig. 1(b)] unless the CC load is connected. The current is determined only by the input voltage; it is independent of the output voltage, because the drain voltage of the SET is kept constant by the MOSFET. When the CC load is connected and the increasing drain current crosses the load line of I_o, the output voltage switches very sharply from high to low. Then, at the second crossing point, it switches from low to high, and so on. Thus, sharp square-wave-like input–output characteristics with a large voltage swing are obtained [Fig. 1(c)]. Note that the CC load can be realized experimentally by using a current-mode output from a semiconductor parameter analyzer with compliance (voltage limit) of V_{dd}. Practically, a depletion-mode MOSFET with its gate and source shorted can be utilized as will be shown later.

Fig. 2(a) is a schematic of the proposed quantizer. Since I_d is independent of V_{out}, the periodic I_d–V_{gs} characteristics of a SET can be converted to two-terminal I_d–V_{out} characteristics by simply connecting the SET gate to the MOSFET drain [Fig. 2(b)]. With a CC load I_o, many stability points appear, and each stability point has a pull-in range separated by the dashed lines. V_{in} fed through the transfer-gate MOSFET is quantized to a stability point after the gate is cut off. This results in the staircase-like V_{in}–V_{out} characteristics shown in Fig. 2(c). This quantizer can be regarded as a static memory as it has a latching capability, i.e., the stable condition is kept even after the input is removed as long as the power is on. The difference between it and our previous MV memory [19] is the addition of the transfer-gate MOSFET. We can directly select any stability points in a short time through this MOSFET.

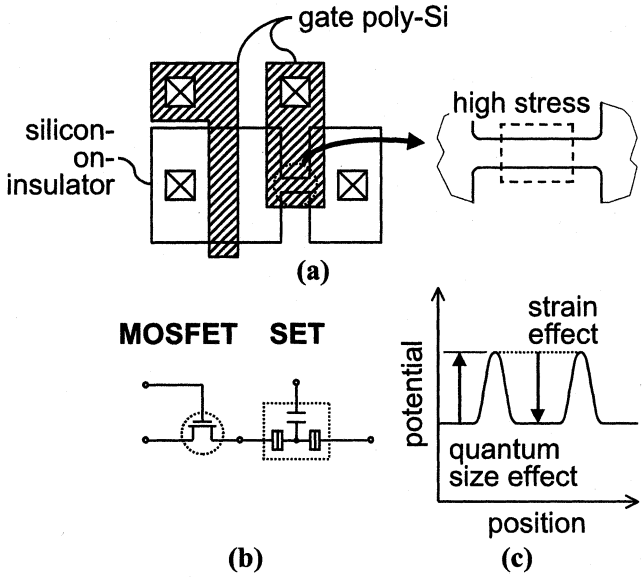


Fig. 3. (a) Possible layout of the integrated SET and MOSFET. (b) Circuit diagram corresponding to the layout above. (c) Potential profile along the length of the narrow wire, where a SET is created by pattern-dependent oxidation (PADOX) [20], [21]. Since areas outside the wire can readily be used for MOSFETs, PADOX is highly compatible with a CMOS process.

Note that the number of periods in the universal literal characteristics [Fig. 1(c)] or voltage levels in the quantizer characteristics [Fig. 2(c)] is infinite in principle. This is a unique feature of our SET-based MV logic, and leads to a considerable reduction of the number of devices in a circuit.

III. Experiments

The layout of the integrated SET and MOSFET, and the corresponding circuit diagram are shown in Fig. 3(a) and (b). Both the

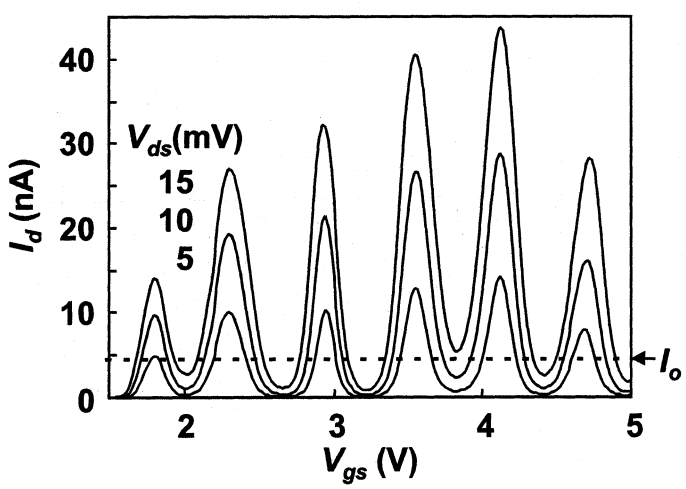


Fig. 4. I_d–V_{gs} characteristics of a SET fabricated by the PADOX process, measured at 27 K.

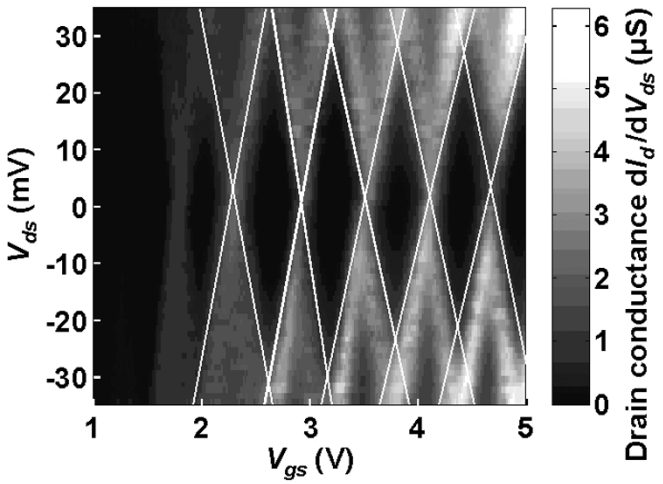


Fig. 5. Coulomb diamond plot of the SET shown in Fig. 4. From this figure, gate capacitance C_g, source capacitance C_s, drain capacitance C_d and tunneling resistance are calculated to be 0.27 aF, 2.7 aF, 2.7 aF and 80∼220 kΩ, respectively.

SET and the MOSFET were fabricated on a thin silicon-on-insulator (SOI) layer whose original thickness before oxidation was 30 nm. The SET was created in a narrow wire region by PADOX [20], [21] at 1000 °C in pure oxygen ambient. The original length and width of the wire were both 50 nm, and the latter shrank to about 10 nm after oxidation. The quantum size effect raises the potential in the wire, but in the middle of the wire the high compressive stress generated by the oxidation reduces the bandgap [Fig. 3(c)] [21]. This creates two tunnel barriers and an island sandwiched between them, which constitute a SET. Since the areas outside the wire can easily be used for MOSFETs, PADOX is highly compatible with the CMOS process.

Fig. 4 shows the I_d–V_{gs} characteristics of a SET with drain voltage as a parameter. Periodic drain-current peaks are clearly seen along with a strong drain voltage dependence of current. As is often observed in semiconductor SETs, the peak heights are uneven and the positions are not perfectly periodic, but the degree of irregularity is acceptable for the following demonstrations of 6-valued operation.

Fig. 5 shows the Coulomb diamond plot for the device shown in Fig. 4. From this figure, gate capacitance C_g, source capacitance C_s, drain capacitance C_d, and tunnel resistance were calculated to be 0.27 aF, 2.7 aF, 2.7 aF, and 80∼220 kΩ, respectively. The maximum voltage gain C_g/C_d (inverting) and applicable voltage e/C_Σ for this SET are as low as 0.1 and 28 mV, respectively. However, there is no problem in constructing the proposed MV logic and memory, because these values are supplemented by the MOSFET.

Fig. 6 shows the subthreshold characteristics of a MOSFET fabricated on the same SOI wafer for drain voltages of 5 V and 10 mV. The gate length and width and the gate oxide thickness are 14 μm, 12 μm, and 90 nm, respectively. In order to maintain the constant drain voltage of the SET, the subthreshold slope of the MOSFET should be steep and the V_{th} shift due to the drain voltage should also be small. The actual subthreshold slopes are 95 and 62 mV/decade for drain voltages of 10 mV and 5 V, respectively, and the V_{th} shift is 53 mV at the drain current of operation (4.5 nA). Despite these rather large values [22], the qualitative behavior of the proposed literal gate and the quantizer can be observed. However, the peak-to-valley current ratios (PVCRs) of I_d in Figs. 1(b) and 2(b) become suppressed, and the ranges of V_{out} in Figs. 1(c) and 2(c) become narrower.

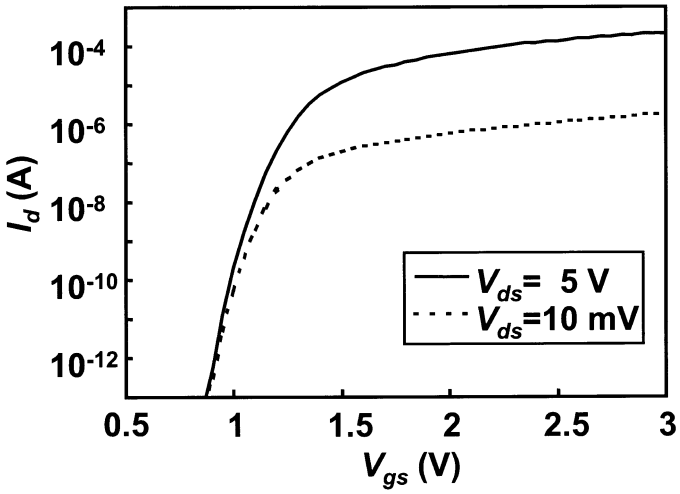


Fig. 6. I_d–V_{gs} characteristics of a MOSFET fabricated on the same SOI wafer as the above SET, measured at 27 K. Effective channel width and length and gate oxide thickness are 12 μm, 14 μm and 90 nm, respectively. Threshold voltage V_{th}, corresponding to $I_d = 4.5$ nA and $V_{ds} = 3$ V, is 1.07 V, and transconductance G_m at $V_{ds} = V_{gs} = 3$ V is 151 μS.

Fig. 7 shows the input–output characteristics of the universal literal gate. The output voltage increases and decreases periodically with the input voltage, reflecting the original characteristics of the SET. The output shows a clear saturation level of as high as 5 V, which is sufficient to drive the next stages of SET or MOSFET circuits. The voltage gain, which represents the sharpness of the transition, is the product of the maximum available voltage gains of the SET and the MOSFET, according to the analysis of a cascode amplifier [23]. If the I_d–V_{ds} characteristics of the MOSFET were perfectly flat in the saturation region, the voltage gain would be infinite and the abrupt transition shown in Fig. 1(c) could be obtained. In reality, the voltage gain of the present MOSFET is only 400, and the resultant slope of the transition is about 40. Though this slope is much larger than the gain of the discrete SET, it still needs further improve-

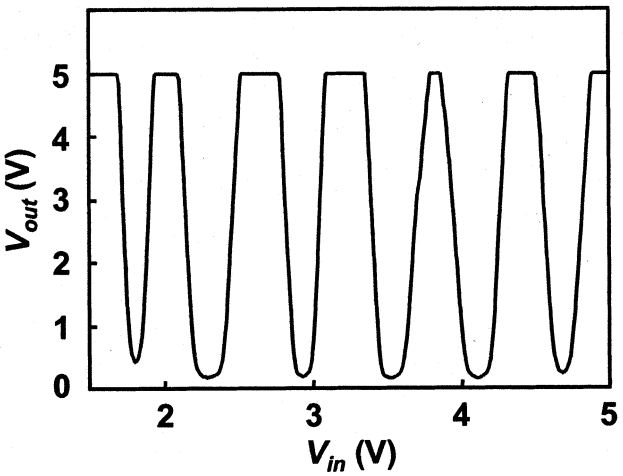


Fig. 7. Measured transfer (V_{in}–V_{out}) characteristics of the proposed literal gate [Fig. 1(a)] comprising a SET, a MOSFET and a CC load. The V_{gg} is set to 1.08 V to attain a SET drain voltage of about 10 mV. The CC load is realized by a current-mode output of 4.5 nA from a semiconductor parameter analyzer with compliance (voltage limit) of 5 V. Originally, the SET I_d–V_{gs} characteristics have a large V_{ds} dependence as indicated in Fig. 4, and this V_{ds} dependence is alleviated by the MOSFET, resulting in a large voltage swing and sharp rises and falls.

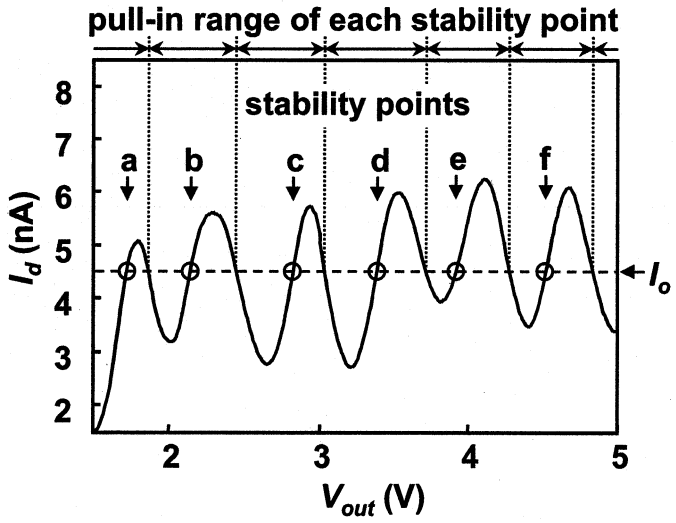


Fig. 8. Two-terminal I_d–V_{out} characteristics of the SET-MOSFET device with the SET gate shorted to the MOSFET drain, measured at 1.08 V of V_{gg} [19]. Stability points ($\mathbf{a}\sim\mathbf{f}$) and the corresponding pull-in ranges expected for the current load of 4.5 nA are also shown.

ment, that could be attained by increasing the output resistance and/or the transconductance of the MOSFET.

Fig. 8 shows the two-terminal I_d–V_{out} characteristics of the SET-MOSFET device with the SET gate shorted to the MOSFET drain [19]. The current increases and decreases periodically, reflecting the I_d–V_{gs} characteristics of the discrete SET. If we were to connect a CC load of 4.5 nA, stability points $\mathbf{a}\sim\mathbf{f}$ corresponding to quantized levels would appear, and each point would have a pull-in range nearly equal to the voltage range of the quantizer input associated with the quantized level. The PVCR of the SET-MOSFET device shown in Fig. 8 is 2.1 at most and much smaller than that of the discrete SET in Fig. 4. This is because the MOSFET is not an ideal constant voltage source to the SET drain; that is, increased drain voltage increases the valley current and decreased drain voltage decreases the peak current. The PVCR can easily be improved to 28 for instance by simply decreasing the C_Σ by a factor of 5 and increasing the tunneling resistance by the same amount [19].

Quantizer operation was verified using the setup shown in Fig. 9. The central SET and MOSFET were on the same wafer, but the transfer-gate MOSFET1 and the MOSFET2 for probing were connected externally. A triangular wave was fed to V_{in}, and the gate of MOSFET1 was driven by short pulses of CLK. Different voltage levels in the triangular wave were sampled by the MOSFET1, transferred to the storage node, V_{out}, and quantized. The waveforms are shown in Fig. 10. V_{out} was quantized to levels $\mathbf{a}\sim\mathbf{f}$ that correspond to stability points in Fig. 8. The operating speed in the figure is not limited by the intrinsic performance of the device, but by the large stray capacitance of 370 pF at V_{out}.

IV. Discussion

A. Application to ADC and MV Adder

Fig. 11 is a block diagram of a 3-bit flash ADC based on the combined SET-MOSFET scheme. Input is quantized by the proposed circuit, and then capacitively divided into the literal gate corresponding to each output digit. Although a conventional n-bit flash ADC requires n^2-1 components, such as comparators, the SET ADC [24], [25] requires only n components. This particular ADC with the quantizer at the front end and the SET-MOSFET literal gates does not require comparators, latches, or ramp generators at each literal gate because the quantizer has a latching capability and the literal gates have square-wave-like transfer characteristics with saturated high and low levels. The use of Gray code is not necessary either, since the quantizer prevents the entry of intermediate voltage levels.

Fig. 12 is a circuit diagram of the ADC in Fig. 11. Depletion-mode MOSFETs are used in place of CC loads ($\mathbf{M3}$, $\mathbf{M5}$, $\mathbf{M7}$ and $\mathbf{M9}$) and to eliminate the gate bias voltage for the stacked MOSFETs ($\mathbf{M2}$, $\mathbf{M4}$, $\mathbf{M6}$ and $\mathbf{M8}$). The MOSFETs for CC loads operate in the saturation region, and the V_{th} or channel width or length must be adjusted to attain the target current I_o. The absolute V_{th} of the stacked MOSFETs, which corresponds to the drain voltage of the SETs, should be low enough to sustain the Coulomb blockade condition.

The circuit shown in Fig. 12 is remarkably simple in that a literal gate is constructed with only three elements and a quantizer with only four. In the conventional implementation with MOSFETs, the main blocks of the ADC, excluding the quantizer, require 28 transistors [8]. The proposed circuit requires only half, i.e., nine transistors and five capacitors.

Fig. 13 shows the block diagram of a full adder for redundant positive-digit number representation PD2-3 [8]. The main parts of this adder are the same as those of the 3-bit ADC in Figs. 11 and 12, and $\oplus$s are the linear sums. This number system is 4-valued, and each digit can take 0, 1, 2, or 3. For example, decimal number 19 can be expressed by $(3, 2, 3)_{PD2-3}$, and 18 can be expressed by $(3, 2, 2)_{PD2-3}$. It can be seen that the sum of these numbers is calculated by this circuit to be $(1, 2, 1, 0, 1)_{PD2-3}$, which corresponds to the decimal 37 and is the right answer. As can be expected from the results for the 3-bit ADC, the number of elements

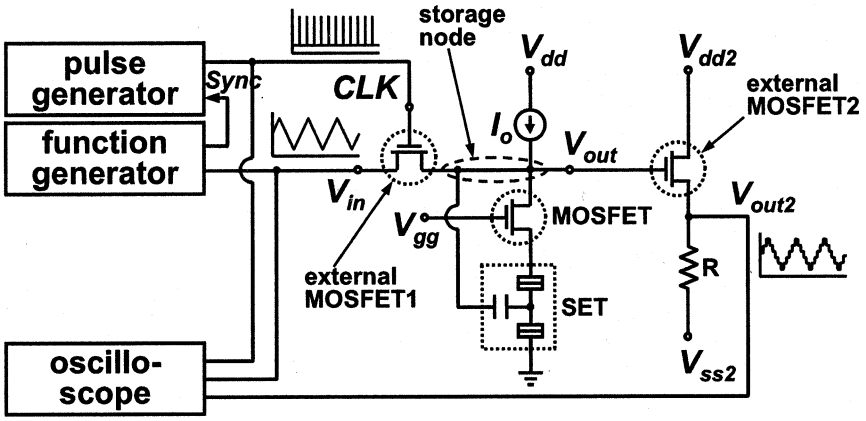


Fig. 9. Measurement setup for the quantizer proposed in Fig. 2(a). The central SET and MOSFET are on the same wafer. The external MOSFET1 is a transfer gate, and MOSFET2 is used as an FET probe to measure the V_{out} sustained by a small current (∼nA).

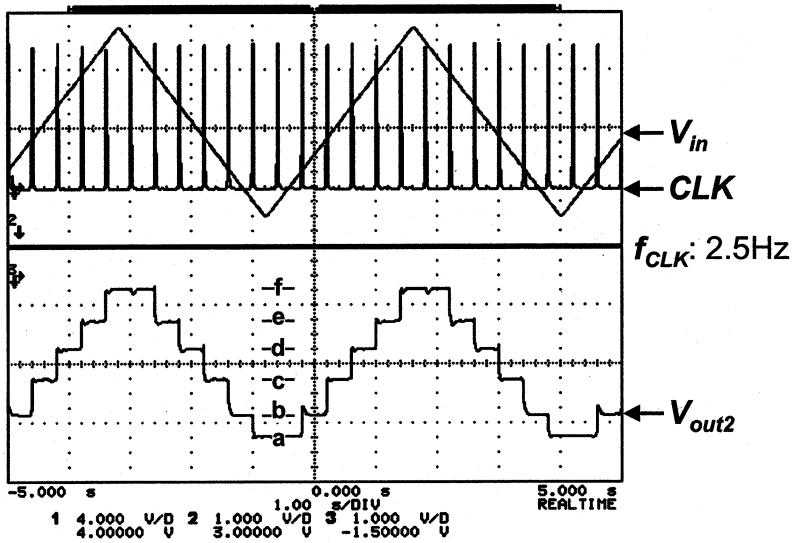


Fig. 10. Quantizer operation measured by the setup in Fig. 9, with V_{gg} of 1.08 V and a CC load of 4.5 nA. Operation speed is not limited by the intrinsic performance of the device, but by the large stray capacitance of 370 pF at V_{out}.

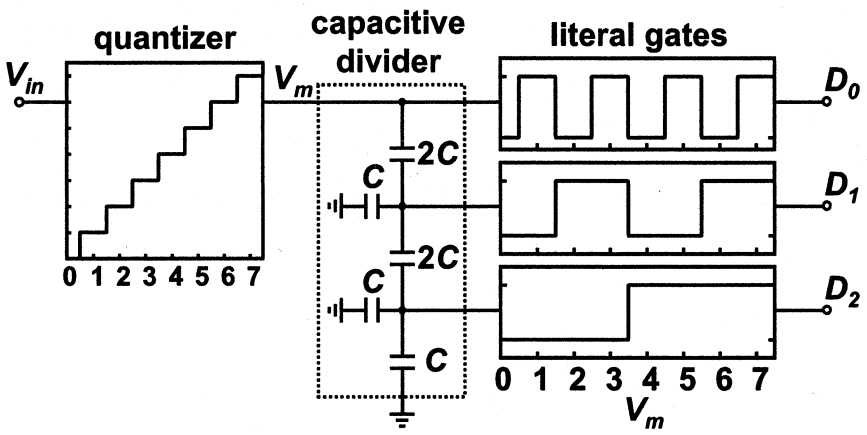


Fig. 11. A block diagram of a 3-bit flash ADC. A conventional n-bit flash ADC requires $n^2 - 1$ components, whereas the SET ADC [24], [25] requires only n. This particular ADC with the quantizer at the front end and with the SET-MOSFET literal gates does not require comparators, latches, or ramp generators at each literal gate. Gray code is not necessary either.

in this adder can be reduced by half through the use of the combined SET-MOSFET scheme. In addition, this multiple-valued arithmetic itself has the merit of high-speed operation due to the elimination of carry propagation.

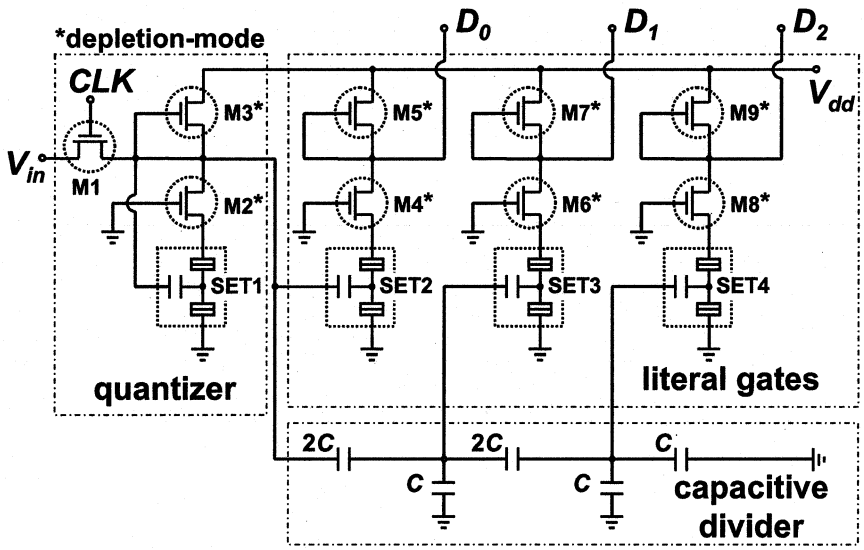


Fig. 12. The circuit diagram of the 3-bit ADC in Fig. 11. Depletion-mode MOSFETs, $\mathbf{M2}$, $\mathbf{M4}$, $\mathbf{M6}$ and $\mathbf{M8}$, keep the drain voltage of the SETs nearly constant at the absolute threshold voltage. Other depletion-mode MOSFETs, $\mathbf{M3}$, $\mathbf{M5}$, $\mathbf{M7}$ and $\mathbf{M9}$, serve as CC loads.

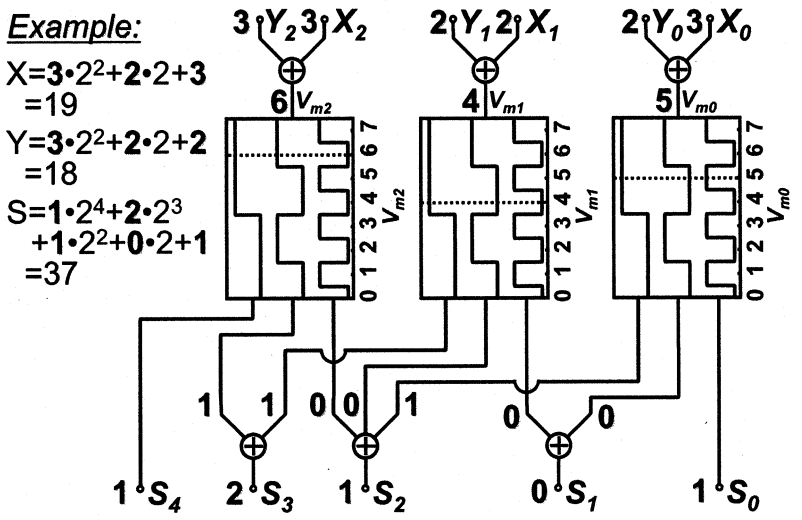


Fig. 13. A full adder for redundant positive-digit number representation PD2-3 [8] consisting of three ADC blocks without a quantizer, and linear sums ($\oplus$). This adder is free from carry propagation, and is thus fast. By using the SET-MOSFET devices, multiple-valued logics of this kind can be made with half the number of elements in conventional implementation.

B. Application to SRAM

Fig. 14(a) shows a four-transistor memory cell for large-scale SRAMs. Again, a depletion-mode grounded-gate MOSFET $\mathbf{M1}$ is used to sustain the SET drain voltage, and another depletion-mode MOSFET, $\mathbf{M2}$, with its gate and source shorted serves as a CC load. The pass-transistor $\mathbf{M3}$ controls the access to the cell. In write operation, the voltage applied to the bit line ($\mathbf{BL}$) is transferred through $\mathbf{M3}$, and is quantized to a stability point after $\mathbf{M3}$ is cut off. In the read operation, the stored voltage level is transferred back to $\mathbf{BL}$ through $\mathbf{M3}$, and then sensed by peripheral circuits. Fig. 14(b) shows an example of the cell layout. The cell has an area of $31.1\boldsymbol{F}^2$, where $\boldsymbol{F}$ is half the minimum wiring pitch. Thus, this cell not only has a multiple-valued capability, but is much smaller than a CMOS binary SRAM cell.

C. Operating Speed

The current that can be supplied from the proposed logic is determined by the margin between the load current $\boldsymbol{I}_o$ and the peak/valley currents, and is of the order of 1 nA (Fig. 8). If we assume the voltage swing of 1 V and the load capacitance of 100 fF, which roughly corresponds to the wiring length of 1 mm, the delay time becomes as large as 100 μs. Since the input capacitance of a SET is very small, the load capacitance can probably be reduced to 100 aF by limiting fan-out and reducing wiring length. The 100 aF is still much larger than the total capacitance $\boldsymbol{C}_\Sigma$ around the Coulomb island, which satisfies the requirement for stable SET operation. The available output current can be increased to over 10 nA by improving the peak-to-valley ratio and adjusting the SET drain voltage. In addition, the voltage swing can be reduced by nearly one

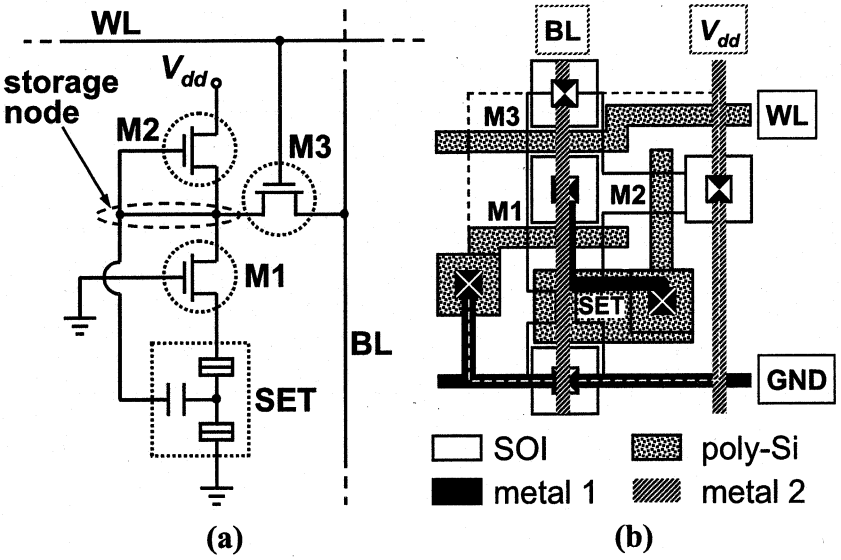
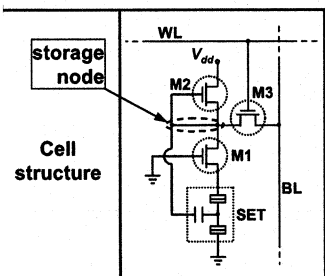
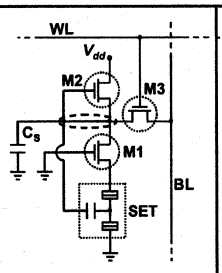
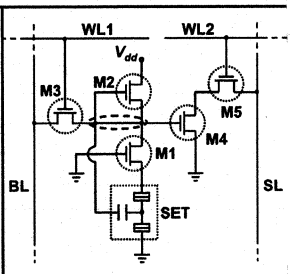


Fig. 14. Single-electron MV SRAM cell with two depletion-mode MOSFETs ($\mathbf{M1}$ and $\mathbf{M2}$) and one enhancement-mode MOSFET ($\mathbf{M3}$). (b) An example of the SRAM layout. Metal-1 and 2 lines are drawn narrower for clarity. The unit cell area surrounded by the dashed line is $31.1F^2$, where F is half the minimum wiring pitch.

TABLE I
CELL STRUCTURES TO IMPROVE THE OPERATING SPEED OF THE MV SRAM

	Original	w/ storage capacitor	w/ read-out Trs.
Cell structure			
No. of elements	4	5	6
Write-in speed	Fast	Fast	Fast
Read-out mode	Non-destructive	Destructive	Non-destructive
Read-out speed	Slow	Fast	Fast
Comparable speed to	—	Multiple-valued DRAM	Multiple-valued Flash

order of magnitude. These changes of parameters would result in a delay time of about 1 ns.

For large-scale memories, different approaches should be taken to improve the speed because the load capacitance, i.e., the $\mathbf{BL}$ capacitance, cannot easily be reduced. Other possible cell structures are compared with the original one in Table I. If we add a storage capacitor C_s to the storage node (center column of the table), the charges stored in C_s can be driven out to the $\mathbf{BL}$ in a short time. The small voltage difference on the $\mathbf{BL}$ is read by a sense amplifier. The speed should be comparable to that of multiple-valued DRAM [26]. Although the read-out operation is destructive, the data would be refreshed immediately by the sense amplifier. Of course, the SRAM proposed above does not require periodic refreshing. Also note that the area penalty due to the storage capacitor is negligible, since the area above the storage node is open in the proposed cell [Fig. 14(b)].

Speed could also be improved by adding MOSFETs specialized for read-out operation (right column of the table). $\mathbf{M4}$ converts voltages at the storage node to current levels, and $\mathbf{M5}$ controls the access from the sense line ($\mathbf{SL}$). By using a special read-out scheme, such as parallel charge sensing, speed comparable to that of MV flash memory [15], [16] could be attained. Although this cell structure enables nondestructive read-out, cell area is sacrificed considerably due to the increased number of transistors.

D. Manufacturing Issues

In the proposed application of a SET to MV logic and memory, control of the oscillation period (e/C_g) and the

threshold voltage is quite important. If the number of MV levels is N, fluctuation of e/C_g should be much smaller than the target e/C_g divided by N, and fluctuation of the threshold voltage should be much smaller than e/C_g. In the PADOX device, we have found a clear relationship between Si wire length and C_g [27]. This means that size control is critical for attaining an accurate oscillation period. We have also found that the threshold voltage of the SET is related uniquely to C_g [28], [31]. This indicates that there is not an apparent effect of random offset charges [29] among the measured devices, and again that size control is crucial for controlling the threshold voltage. Since the densities of interface traps and fixed oxide charges in the Si–SiO_2 system are of the order of 10^{10} cm^{-2}, we cannot ignore the random offset charges in large-scale circuits. Still, the primary concern in the present device is size control. Considering the rapid progress of Si LSI technology [30], we will be able to attain a better control of size and to make SET-MOSFET hybrid circuits with predetermined characteristics in the foreseeable future.

V. Conclusions

We made the best use of the periodic nature of the SET characteristics to construct MV logic and memory. By combining a SET with a MOSFET, which can be fabricated on the same SOI wafer by the PADOX process, we obtained a universal literal gate that has sharp transfer characteristics and large output amplitude. We also verified the operation of a novel quantizer, which is equivalent to a MV static memory, based on the same scheme. These basic components for MV logic and memory are extremely compact in that the literal gate requires only three elements and the quantizer only four. Moreover, the number of periods or quantized levels is infinite in principle and does not affect the circuit size. With these components, we showed that a 3-bit flash ADC and a carry-propagation-free adder for redundant number representation PD2-3 could be made with half the number of elements in a conventional implementation. A MV SRAM cell could be made with an area of $31.1F^2$, which is much smaller than that of a CMOS binary cell. These results open up the possibility of constructing a new class of MV logic and memory with single-electron devices.

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