A Study on Column-Parallel Low-Noise Readout Circuits for CMOS Image Sensors

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This thesis is focused on column-parallel low-noise readout circuits for CMOS image sensors. Amplification at the column-parallel signal readout circuits is effective for reducing the readout noise of CMOS image sensors. However, the simple amplification leads to the reduction of signal dynamic range. This thesis treats three techniques for reducing the readout noise while maintaining the wide dynamic range.

The first technique proposed is an adaptive amplification of image signal. Using a comparator in each column, pixel output signal is adaptively amplified with the gain of 1 or 8. An experimental application of the circuit using 0.25μm CMOS technology with pinned photodiodes gives a low random noise of 263μVrms and a wide dynamic range of 71dB.

The second technique uses an analog-to-digital converter for low-noise signal readouts and the wide dynamic range in digital domain. The proposed digital double integration with a delta modulation type A/D converter effectively reduces both the random noise and the quantization noise. The quantization noise reduction effect is theoretically analyzed with a state transition diagram and is confirmed by simulations with random signals.

The third technique is based on an adaptive integration for effective noise reduction and the resulting wide dynamic range in digital domain. Experimental results show that the column adaptive integration of 16 times and succeeding 12-bit cyclic A/D conversion attain the random noise of 66.1μVrms and linear dynamic range of 82.7dB.