# Signal integrity analysis and its applications for board level circuit design

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This thesis describes the simulation techniques for signal integrity analysis in board level circuit design. It starts with the background that indicates the necessity of efficient simulation techniques. After the introduction, Chapter 2 describes the simulation technique with the reduced-order model. The reduced-order model that is obtained by the linear circuit reduction technique, PRIMA, is modeled as a voltage controlled current source and high-speed simulation is performed. In addition, the model order reduction technique for nonlinear circuits is described in Chapter 3. The proposed method improves the generation of projection matrix and reduced Jacobian. Then, this method enables the fast simulation for arbitrary circuits. In Chapter 4, FDTD method is applied to the signal integrity analysis for microstrip line and the accuracy and efficiency of the method is estimated. The value of characteristic impedance in FDTD simulation, which is related with cell size, is estimated by FDM. Also, what-if analysis for the multi-layer PWB is demonstrated with parallel and distributed FDTD based simulator. In Chapter 5, the enhanced time-domain circuit simulation method based on LIM latency insertion method is suggested. LIM has the limitation of the circuit structure to be analyzed. The proposed method is applicable to any structure of circuits by combination with the SPICE-like method. It is expected that these techniques are useful for the verification of power / signal integrity.