

Transient Simulation of Lossy Transmission Lines and Bipolar LSI Circuits Based on Waveform Relaxation Approach

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In this thesis, we primarily focus on the transient analysis of lossy transmission lines based on waveform relaxation approach and extend the method with the aim of improving the simulation efficiency. It is observed that synthesized model of characteristic impedance, which adds several nodes to each subcircuit, becomes the dominating factor in the over all simulation time. Assuming that the application is limited to digital circuits, we proposed a simplified characteristic impedance model and established the criteria under which such a model should be switched in. The simulated waveforms exhibit increasing period of latency with successive waveform relaxation iterations, in steps of twice the transmission line delay. A method is established to determine the interval of waveform latency in each iteration which helps in skipping the simulation in that interval. Waveform relaxation normally requires several iterations for satisfactory convergence, especially so with low loss transmission lines. This problem is addressed by a novel 'line delay window' algorithm, which exploits the inherent delay of the transmission line. In effect, the new algorithm is equivalent to obtaining the converged waveforms with a single iteration. This 'line delay window' algorithm is extended for the case of coupled lines with the assumption that the lines are identical and equally spaced.

High speed digital circuits employ emitter coupled logic (ECL), which are made up of bipolar transistors. Application of waveform relaxation technique for such circuits is not easy and usually require special partitioning techniques. One way of performing the system decomposition is to carry out partitioning at each metal interconnection. However, such a scheme has convergence problems for the case of interconnects which almost behave like short circuits. As a secondary objective of this thesis we focussed on alternative partitioning schemes for the case of bipolar circuits. Two new partitioning schemes, based on gate level partitioning and dynamically overlapped partitioning, are presented which are found to be very useful for the case ECL, bipolar circuit simulation.