TRANSIENT SIMULATION OF LOSSY TRANSMISSION LINES AND BIPOLAR LSI CIRCUITS BASED ON WAVEFORM RELAXATION APPROACH

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論文内容の要旨

The interconnects in high-speed and high-density digital circuits behave like lossy transmission lines, causing unwanted effects such as delay, reflections, cross talk, dispersion and so on. Therefore, when such circuits are simulated, it is very essential to treat the interconnects as distributed transmission lines. The fundamental difficulty, encountered in integrating transmission line simulation into transient simulator, arises because circuits containing nonlinear devices or time-dependent characteristics must be characterized in time domain while transmission lines are best characterized in the frequency domain.

Among the other possible solutions to the above problem, the waveform relaxation based approach in conjunction with the characteristic model, which was proposed by F.Y.Chang, is very attractive because of two reasons. Firstly, Pade synthesis of characteristic impedance and exponential propagation functions make it possible to carry out the simulation entirely in time domain. Secondly, characteristic model enables easy implementation of waveform relaxation scheme by virtue of simplified partitioning process (since each metal connection becomes a natural boundary for system decomposition) and favorable convergence property. When a very large scale integrated (VLSI) circuit is simulated, waveform relaxation is desirable due to its high efficiency when compared with

the direct method.

In this thesis, we focus on the transient analysis of lossy transmission lines based on waveform relaxation approach and extend the method with the aim of improving the simulation efficiency. It is observed that synthesized model of characteristic impedance, which adds several nodes to each subcircuit, becomes the dominating factor in the over all simulation time. Assuming that the application is limited to digital circuits, we proposed an acceleration technique based on simplified characteristic impedance model and established the criteria under which such a model should be switched in. This is equivalent to choosing a higher order approimation when the signals are changing rapidly and selecting a lower order approximation otherwise. When a large circuit is simulated, at any given interval of time, typically a small % of the circuit is very active and the rest of it is so inactive that a simplified approximation (characteristic impedance model) is adequate. Furthermore, it is shown that higher the ratio between the load impedance and the characteristic impedance of the line, higher the % of simulation interval during which the simplified characteristic impedance model is valid. This implies that when a line is terminated with high impedance loads, such as ECL gates, the present acceleration technique speeds up the overall simulation very significantly. Out of the two possible lumped element models, which represent the exponential propagation function, we have identified the model made up of resistive and inductive elements to be preferabel from the simulation efficiency point of view. A new method of computing current waveforms, using this model, has been formulated which neither requires nodal analysis nor time consuming matrix inversion.

The second acceleration technique, presented in this thesis, is based on the exploitaion of increasing period of waveform latency with successive waveform relaxation iterations, in steps of twice the transmission line dalay. A method is established to determine the interval of waveform latency in each iteration which helps in skipping the simulation in that interval.

Waveform relaxtion normally requires several iterations for satisfactory convergence, especially so with low loss transmission lines. This problem is addressed by a novel 'line delay window' algorithm, which exploits the inherent delay of the transmission line. In effect, the new algorithm is equivalent to obtaining the converged waveforms with a single iteration. It is shown that if terminal waveforms and waveform generator waveforms (reflected waveforms) are known in a time window of size equal to or greater than the line dely, then it is possible to compute the waveform generator waveforms corresponding to the next time window. This ability of computing the waveforms of the waveform generators s the basis of the 'line delay window' technique. The validity of 'line delay window' algorithm is extended for the case of lossy coupled lines. Assuming that the coupled lines are identical and equally spaced, first, the coupled system is decoupled using a transformation matrix which is a function of only the number of lines, second, each uncoupled line is modelled into characteristic form. Window size is made equal to the delay of one of the uncoupled lines which represents the fastest wave propagation mode.

High speed digital circuits employ emitter coupled logic (ECL), which are made up of bipolar transistors. Application of waveform relaxation technique for such circuits is not easy and usually require special partitioning techniques. One way of performing the system decomposition is to carry out partitioning at each metal interconnection. However, such a scheme has convergence problems for the case of interconnects which almost behave like short circuits. In such cases, alternative partitioning schemes, based on gate level partitioning and dynamically selected overlapped partitioning, have been investigated, The first method is very promising as an efficient timing sumulator, while the second method is preferable where the simulation accuracy is important.

論 文 審 査 結 果 の 要 旨

本論文では、ディジタルバイポーラトランジスタ回路系の波形緩和解析手法について述べている。

第2、第3章では、損失伝送線路を含む回路の波形緩和法に基づく過渡解析手法について述べ、その高速化手法についてのいくつかの提案を行っている。第2章では伝送線路を含むディジタル回路の解析に対して、簡単化された特性インピーダンスモデルが提案される。また、ディジタル信号を入力とする場合、回路の潜在性が利用でき、提案モデルの導入により、波形緩和解析が効果的に利用できることが示される。

波形緩和法では、通常、幾度かの反復計算により過渡解を求めることになり、その収束性を改善するために解析区間が窓と呼ばれる幾つかの時間領域区間に分割される。第3章では、伝送線路の解析において信号の反射を考慮した窓幅の決定法についての提案を行っている。本手法によれば、緩和反復無しに極めて精度の高い過渡解が得られることが示される。本手法を単相線路および多相線路の解析に適用することにより、その有効性を検証している。

通常、波形緩和法は比較的非線形特性が緩やかなMOS(Metal Oxide Semiconductor)トランジスタ回路系に適用される。第4章では、特に、高速動作を必要とするECL(Emitter Coupled Logic)バイポーラ回路で駆動される回路系を扱っている。MOSトランジスタ回路系では、静的回路分割により高速化が実現されるのに対し、ECLで駆動される集中定数系回路に対して、緩和法の適用を可能にするための動的重複回路分割手法についての提案を行っている。

更に、第5章において、バイポーラディジタル回路の解析に対してはゲート回路レベルでの分割が波形緩和解析に有効であることを示している。

以上、本論文においては、バイポーラトランジスタ回路を含む集中定数系および分布定数系の回路に対する波形緩和解析を高速化するための幾つかの提案を行い、その有効性を検証している。

以上の成果は回路シミュレーション分野を中心として工学的に価値があり、博士の学位を与えるにふさわしい内容を持つものと認定する。