Study of New Fabrication Technique for GaAs Static Induction Power Devices

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GaAs Static Induction (SI) power devices have several excellent device performances. However, GaAs process technology is not so far advanced compared to Si's, and very few works have been reported on the SI devices of GaAs.

In this study, the development of the new fabrication technique for GaAs SI power devices was investigated.

At first, the properties of undoped liquid phase epitaxial (LPE) GaAs layers grown at various growth conditions were investigated to attain low impurity (high purity) epitaxial layers.

Next, numerical simulation of GaAs pin diode which forms fundamental part of SI devices and of which the characteristics is directly related to those of SI devices was carried out.

A new fabrication technique to form the junction between a low impurity layer and a high impurity layer using LPE based on the concept of inverse epitaxy and lattice compensation effect was developed.

GaAs pin diodes with the junction that was formed using the new fabrication technique were fabricated and examined. In this stage, LEC (liquid Encapsulated Czochralski) undoped semi-insulating GaAs wafer was used as a low impurity layer in the junction.

Then this new fabrication technique has been applied to fabrication of GaAs p-channel BSIT. The current gain of our device is poor but it is clearly indicated that the bipolar mode operation occurred.

Furthermore, a newer fabrication technique combined high purity LPE growth technique and inverse epitaxy technique was proposed.